A Boosted Wordline Voltage Generator for Embedded Low-Voltage Memories *

Chua-Chin Wang†, *Ya-Hsin Hsueh, Ting-Wan Kuo* ‡, *and Ron Hu* §
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Tel : 886-7-5252000 ext. 4144
Fax : 886-7-5254199
Email : ccwang@ee.nsysu.edu.tw

Abstract

A novel voltage tripler using 4 clocks with different phases is presented in this work. Both the positive and negative polarities of the voltage are generated to serve as the boosted voltage and the back bias voltage. The proposed design is carried out by pass transistors and switched capacitors. The largest generated voltages which the proposed design can provide is +11.09 V and -10.62 V given VDD = 3.3 V when the circuit is implemented by TSMC 0.35 μ 1P4M CMOS technology.

Key words : BVG (boosted voltage generator), memory devices, BBG (back bias generator), programming voltage

Name of Workshop : **Computer Systems**

*This research was partially supported by National Science Council under grant NSC 89-2215-E-110-017 and NSC 89-2215-E-110-014.

†The contact author
‡Mr. Kuo is Product Engineer of Wafer Testing Factory of Philips Semiconductors Kaohsiung, Taiwan.
§Dr. Ron Hu is the General Manager of Asuka Semiconductor Inc., Taiwan.

1 Introduction

Charge pumps play an important role in memory designs. They are also used for low-voltage volatile memories, e.g., DRAM and SRAM for boosting word line voltage to compensate the threshold voltage of the MOS or boosting bit line voltage to raise the speed of readout operations [1], [3]. Owing to the presence of the threshold leakage and the body effect of MOS transistors, the pumping gain of prior charge pump designs has been a problem to be resolved. It is particularly crucial when ultra low-voltage embedded memory IP's (intellectual property) are integrated with CMOS circuits in SOC (system-on-chip) designs. Most of the prior works were focused on the generation of a positive high voltage [2], [4], [5], [6], [7], [8], [10]. By contrast, a negative high voltage is often required for the back bias which is used to reduce the sub-threshold current and junction capacitance. The negative voltages produced by a back bias generator (BBG) can be used to enhance the device isolation capability and the latch-up immunity [1]. In this paper, we present a novel charge pump design, which utilizes only pass transistors and capacitors, to generate both positive and negative voltages. The highest output voltage is ± 3 times of the supplied voltage, VDD, given that VDD is as low as 1.5V.

2 Dual-Polarity Charge Pump

We will introduce the design of a BVG (boosted voltage generator) which is a positive voltage tripler. Then, a BBG which is a negative voltage tripler is discussed. A final combination of the BVG and the BBG, i.e., the dual-polarity charge pump, is revealed at last.

2.1 Boosted voltage generator

The proposed voltage tripler is shown in Fig. 1. There are a total of three pumping stages which are driven by four different clocks, clk1, clk2, clk3, and clk4. The clocking scheme is summarized as follows.

1). The $1 \rightarrow 0$ transition of clk2 must occur before the $0 \rightarrow 1$ transition of clk1. Besides, the next $1 \rightarrow 0$ transition of clk1 must take place before the $0 \rightarrow 1$ transition of clk2. Otherwise, either violation of the mentioned two requirements will cause leakages via pass transistors. The required clocking waveforms are shown in Fig. 2.

2). The amplitude of the clocks is equal to the voltage of the given VDD.

3). The clk3 and clk4 are lagged the clk1 and the clk2 by 90^o, respectively, to ensure the correctness of the circuit.

4). Capacitor, C_i, is coupled with the gate of NMOS pass transistor NM_i, $\forall i = 1, \ldots, 6$, to add one VDD voltage to the output voltage.

5). Theoretically, a pumping stage is composed of 2 NMOS pass transistors and 2 switched capacitors, e.g., NM_1, NM_2, C_1, C_2.

6). The number of states constructed by the four clocks is 6. These six states constitutes a cycle which will repeat as long as the clocks sustain. The output voltage will then converge to a stable state.

It is obvious that the proposed design is basically using a 2-clock scheme, which is much simpler than the prior 4-clock schemes [6], [7]. Meanwhile, the same design methodology can be applied to a higher voltage generator by increasing the amplitude of clk1 and clk3 [11] or adding more pumping stages to the one in Fig. 1.

2.2 Back bias generator

By applying the same design methodology, the BVG in previous section can be modified to be a back bias generator which provides a negative voltage source. There are also a total of four pumping stages which are driven by four different clocks, $\overline{\text{clk1}}$, $\overline{\text{clk2}}$, $\overline{\text{clk3}}$, and $\overline{\text{clk4}}$, which are the inverse waveforms in Fig 2. The operation of the proposed BBG, which is shown in Fig. 3, is summarized as follows.

1). By a dual design concept, all of the NMOS transistors are substituted with PMOS transistor, which are labeled as $PM_1, \ldots, PM_9$. It is noted that the pumping stages are 4 in the proposed BBG due to the intrinsically poor current switching capability of PMOS transistors.

2). All of the clocks are exactly out of phase with respect to those in the BVG design.

3). The input of the first pumping stage is GND instead of VDD which is the input of the first pumping stage in the BVG design.

4). Theoretically, a pumping stage is composed of 2 PMOS pass transistors and 2 switched capacitors, e.g., $PM_1, PM_2, C_{P1}, C_{P2}$.

Similarly, the same design methodology can be applied to a higher voltage BVG by adding more pumping stages to the one in Fig. 3.

2.3 Dual-polarity voltage generator

Since the BVG and the BBG described in the previous two sections are completely dual designs, their combination is feasible by using inverters to

generate two groups of out-of-phase clocks. The entire dual-polarity voltage generator is given in Fig. 4.

3 Chip Implementation & Simulation

Fig. 5 shows the post-layout simulation results of our design by TimeMill. The proposed design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 1P4M CMOS technology, and the die photo is shown in Fig. 6. Comparison of our design with Dickson [12] and NCP-2 (charge pump using dynamic charge transfer switches) [10] are shown in Fig. 7 and Fig. 8. The loading capacitor is 20 pf, and clock period is 80 ns. The overall performance of the proposed charge pump tabulated in Table 1. The overall comparison for the boosted voltage generator are shown in Fig. 9, and Fig. 10. Fig. 11 is the comparison of pumping stages vs. output voltage in different designs.

The output of every pumping stage of Dickson decreases one Vth. Therefore, the final output of this charge pump is reduced by (# of the pumping stage)·(Vth) volt. Besides, parasitic capacitance of the NCP-2 design is 3 times of that of Dickson's design, which deteriorates the pumping efficiency [10]. Hence, our design outperforms these two prior works, because of the special 4-clock scheme.

4 Conclusion

In this paper, a novel dual-polarity charge pump design, which utilizes only pass transistors and capacitors, is presented to generate both positive and negative high voltages to serve as boosted voltage and back bias of

input VDD	V_{out_P}	V_{out_N}
1.5	3.2	-2.32
2.5	7.11	-6.10
3.3	11.09	-10.62
4.0	13.68	-14.04
5.0	15.89	-17.7

Table 1: Simulation summary of the proposed design (unit = volt)

memory devices. The simulated results also show the performance of our design is better than others.

References

[1] A. Bellaouar, and M. I. Elmasry, "Low-power digital VLSI design - ciucuits and systems," Reading: Kluwer Academic Publishers, 1995.

[2] I.-Y. Chung, Y. J. Park, and H. S. Min, "A charge pumping device with a potential barrier using inversion charge transfer," *IEEE Trans. on Electron Devices,* vol. 48, no. 6, pp. 1216-1221, June 2001.

[3] T. P. Haraszti, "CMOS memory circuits," Reading: Kluwer Academic Publishers, 2000.

[4] S.-W. Kwack, S.-H. Lee, J.-D. Joo, B.-G. Ko, B.-G. Song, J.-G. Park, and K.-D. Kwack, "A novel substrate-bias generator for low-power and high-speed DRAMs," *Proceedings of the IEEE Region 10 Conference (TENCON 99),* vol. 2, pp. 864 -867, 1999.

[5] Y.H. Kim, J.K. Nam, Y.S. Sohn, S.C. Heo, S.H. Lee, H.J. Park, Y.S. Han, J.I. Doh, Y.J. Choi, J.H. Choi, J.S. Choi, and C.S. Park, "Two-

phase boosted voltage generator [CMOS DRAMs]," *6th International Conference on VLSI and CAD (ICVC'99),* pp. 586-589, 1999.

[6] H. Lin, and N.-H. Chen, "New four-phase generation circuits for low-voltage charge pumps," *2001 Inter. Symp. on Circuits and Systems,* vol. 1, pp. 504-507, May 2001.

[7] H. Lin, and N.-H. Chen, "An efficient clock scheme for low-voltage four-phase charge pumps," *2001 Inter. Symp. on VLSI Technology, Systems, and Applications,* pp. 228-231, 2001.

[8] K.-S. Min, and J.-Y. Chung, "A fast pump-down V_{BB} generator for sub-1.5-V DRAMs," *IEEE J. Solid-State Circuits,* vol. 36, no. 7, pp. 1154-1157, July 2001.

[9] B. Prince, "Semiconductor memories," Reading: John Wiley & Sons Ltd., 1991.

[10] J.-T. Wu, and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE J. Solid-State Circuits,* vol. 33, no. 4, pp. 592-597, Apr. 1998.

[11] Park, *al.*, "High voltage charge transfer stage," Patent 5886566, Mar. 1999.

[12] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits,* vol. 11, no. 3, pp. 374-378, 1976.

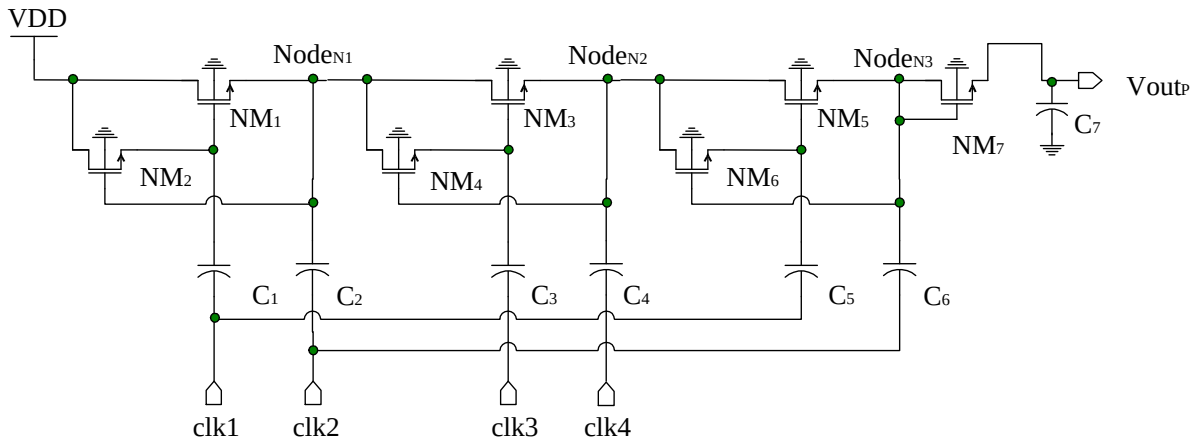

Figure 1: Proposed charge pump for the BVG design

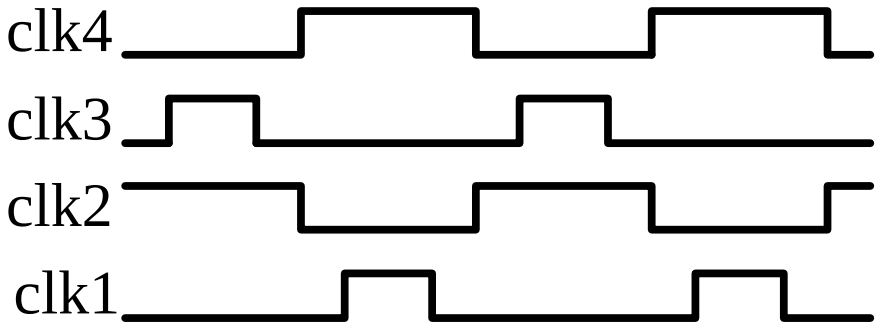

Figure 2: 4-phase clocking scheme for the BVG

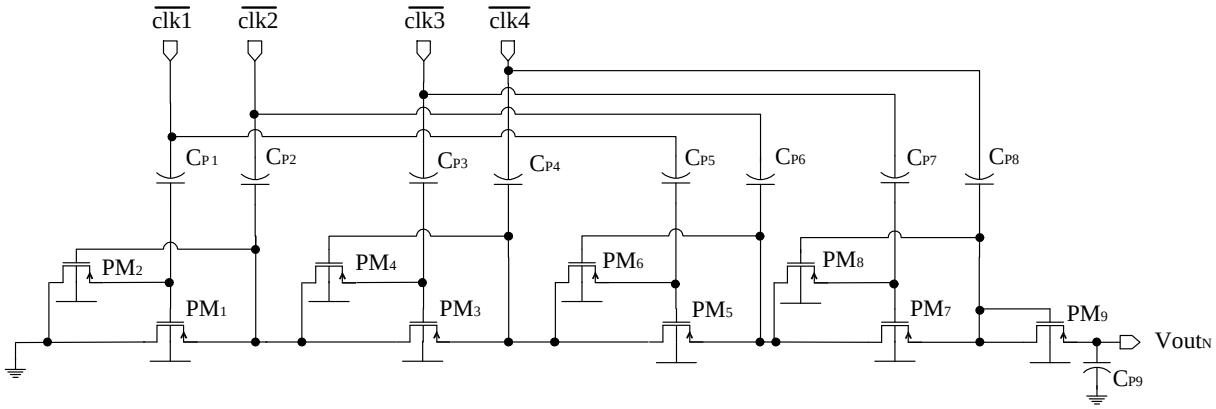

Figure 3: Proposed charge pump for the BBG design

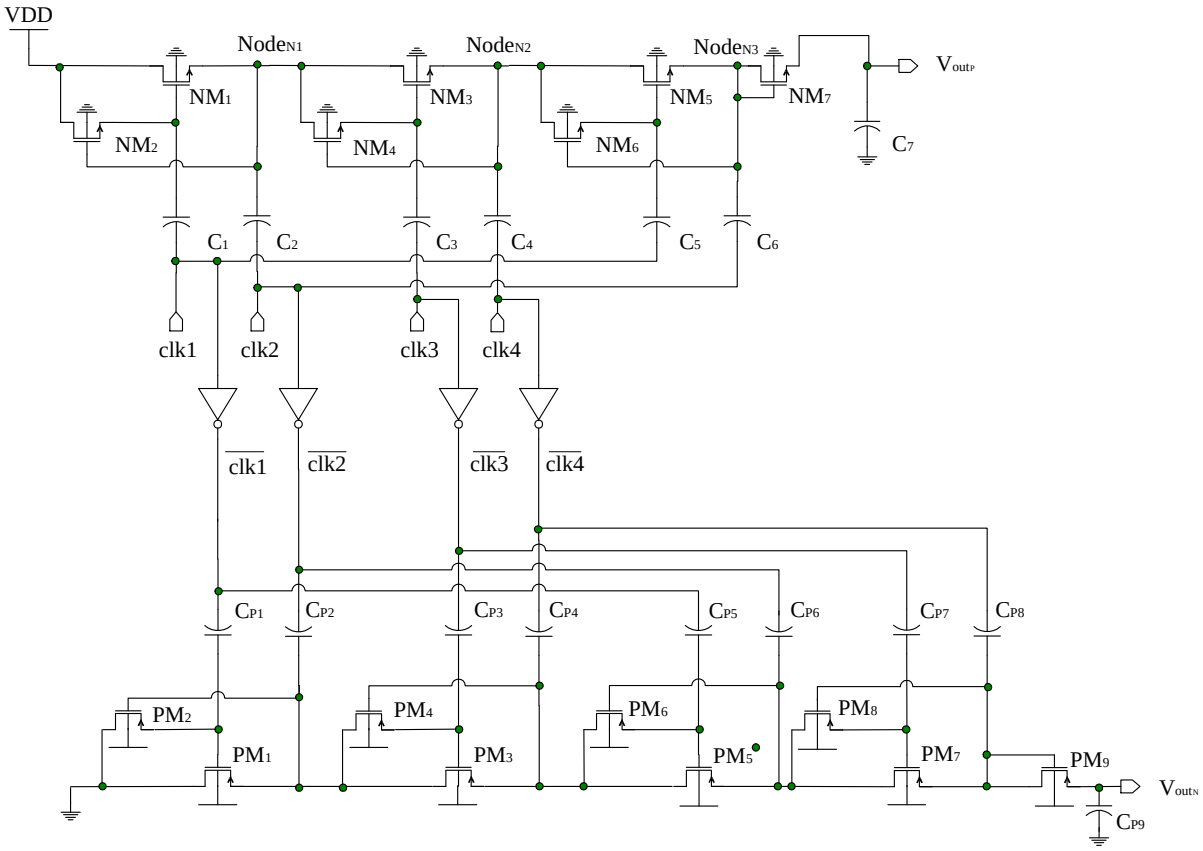

Figure 4: Proposed dual-polarity voltage generator

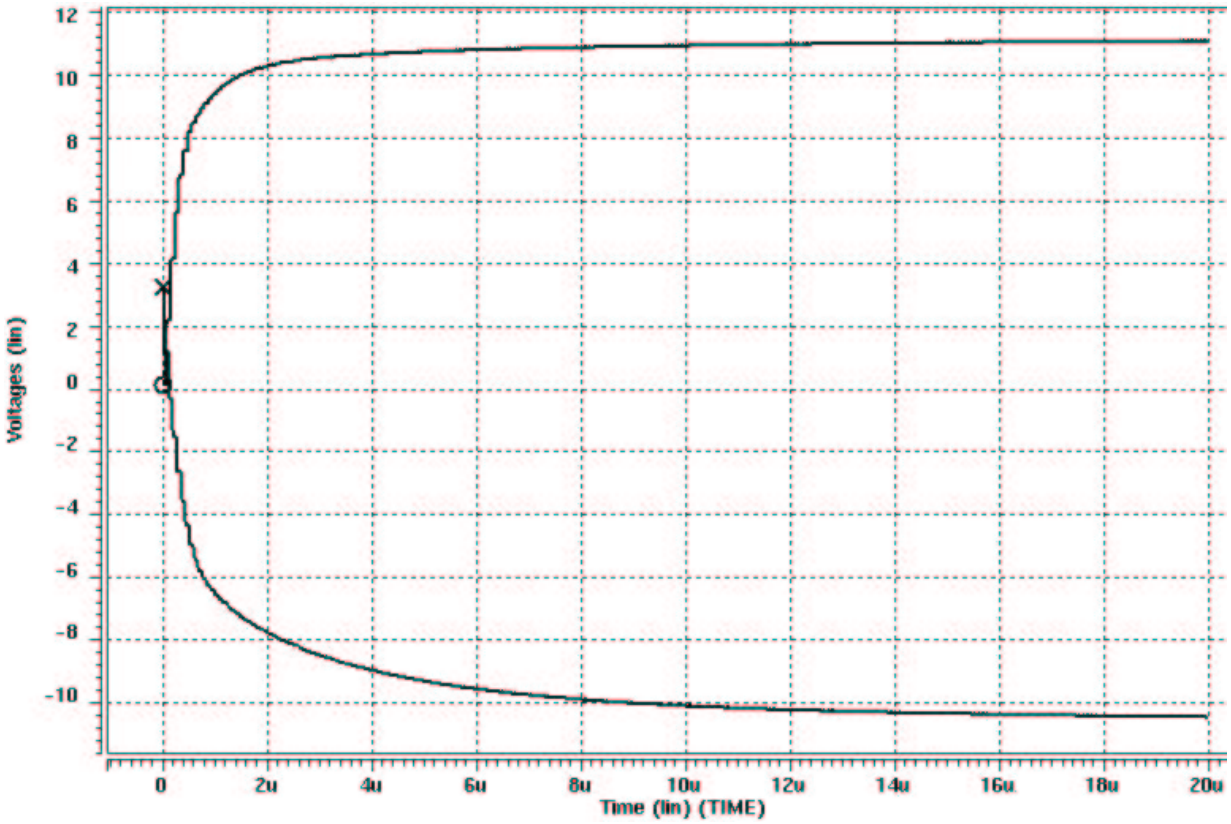

Figure 5: Post-layout simulation (25^{o}C, TT mode, input=3.3V)

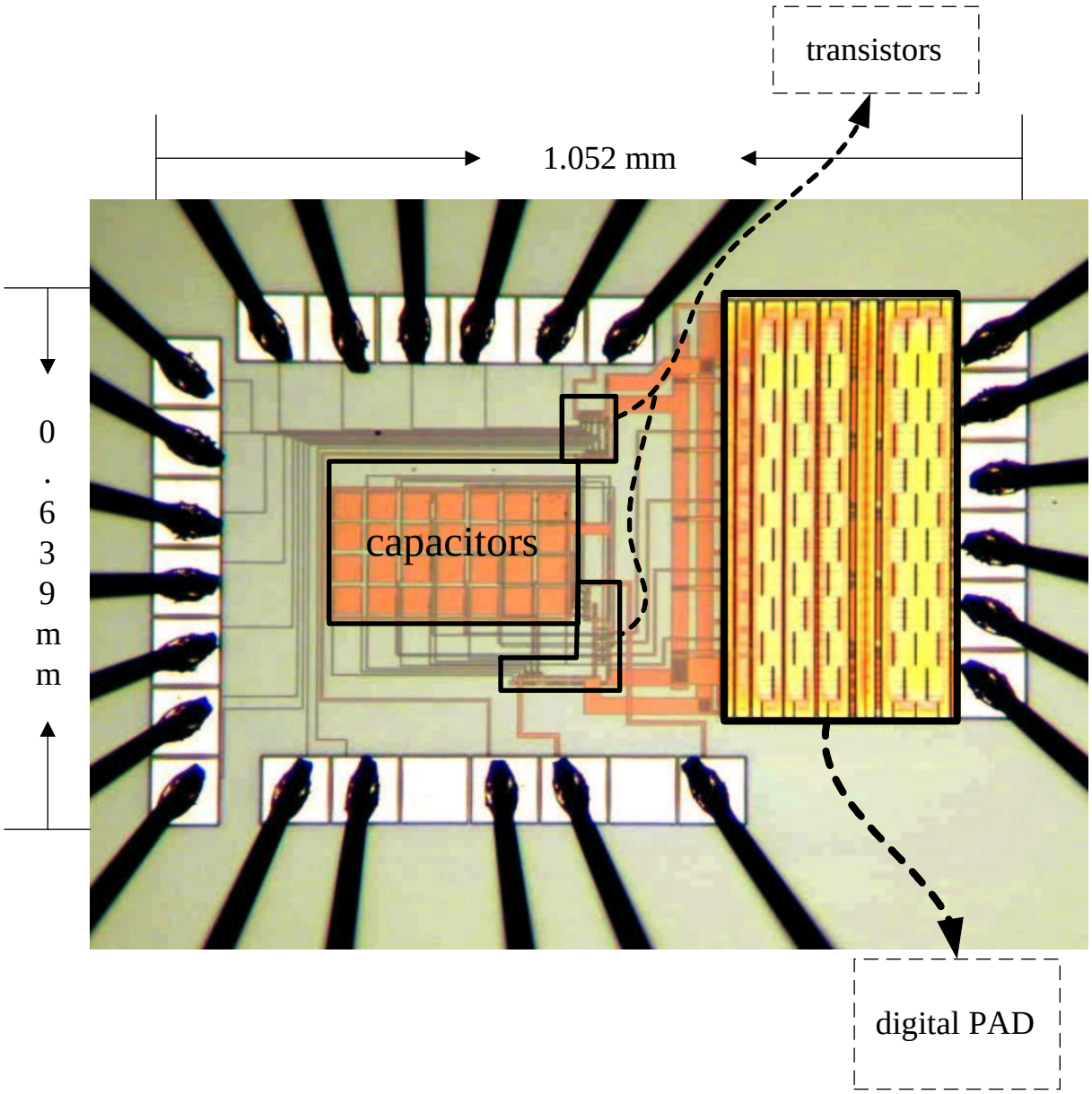

Figure 6: Die photo of the design

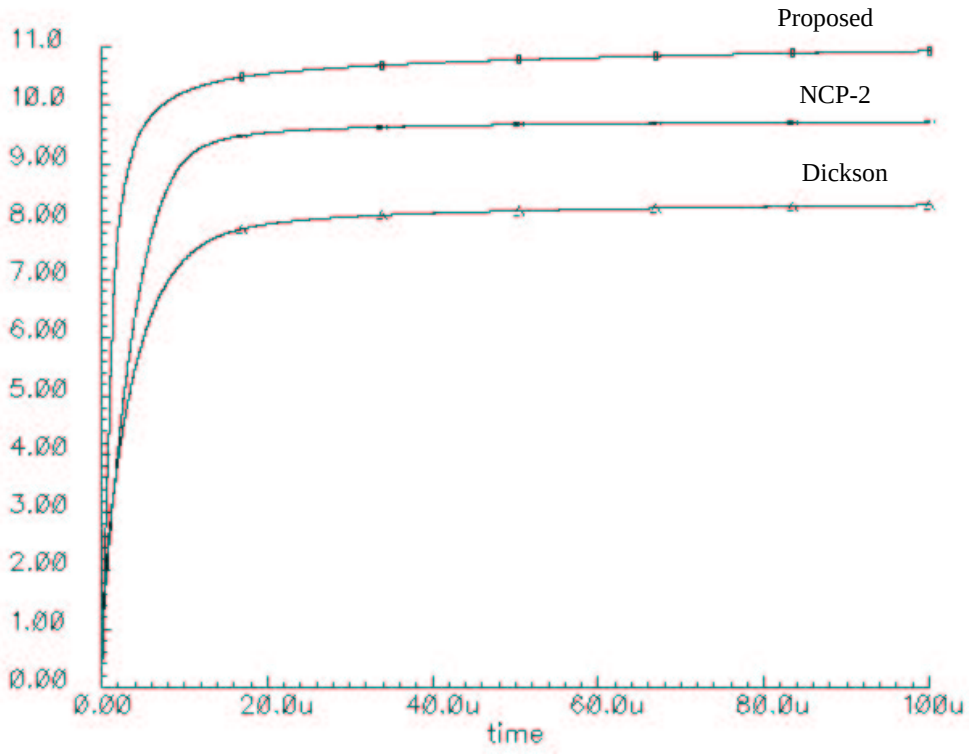

Figure 7: Output voltage comparison given a 3.3V input

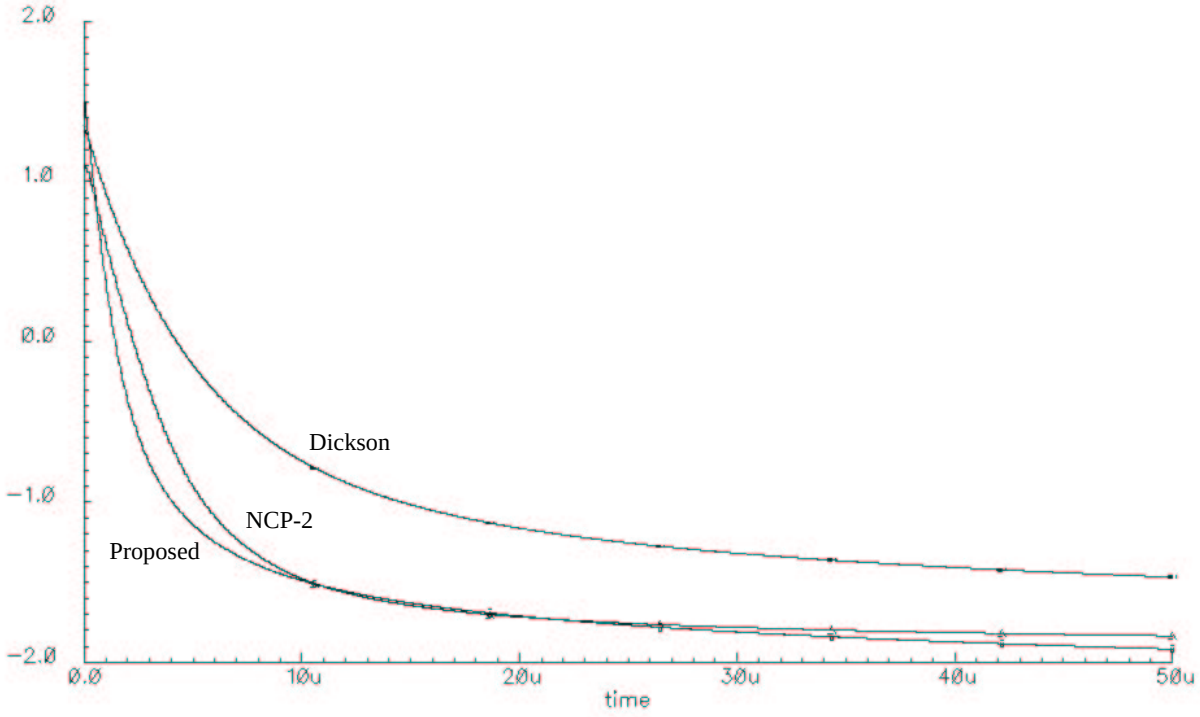

Figure 8: Output voltage comparison given a 1.5V input

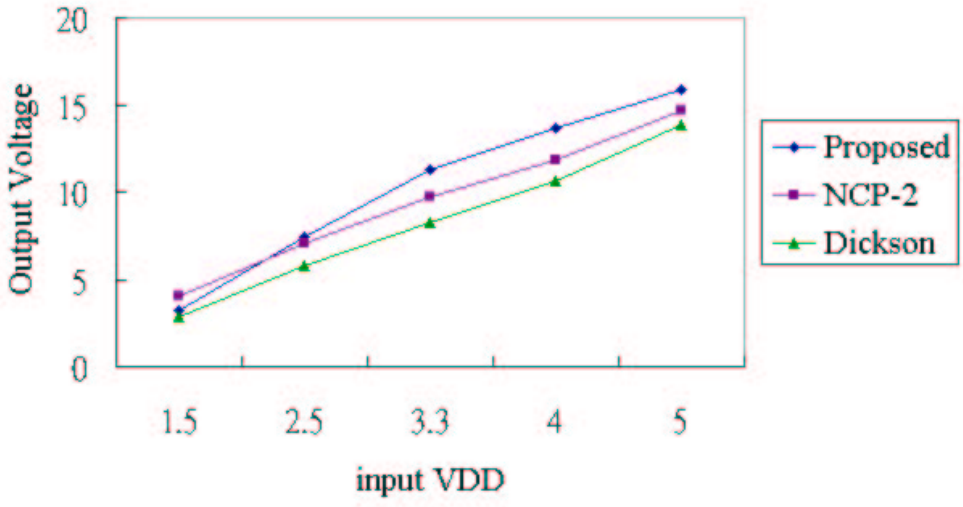

Figure 9: Input VDD vs. output voltage in boosted voltage generator

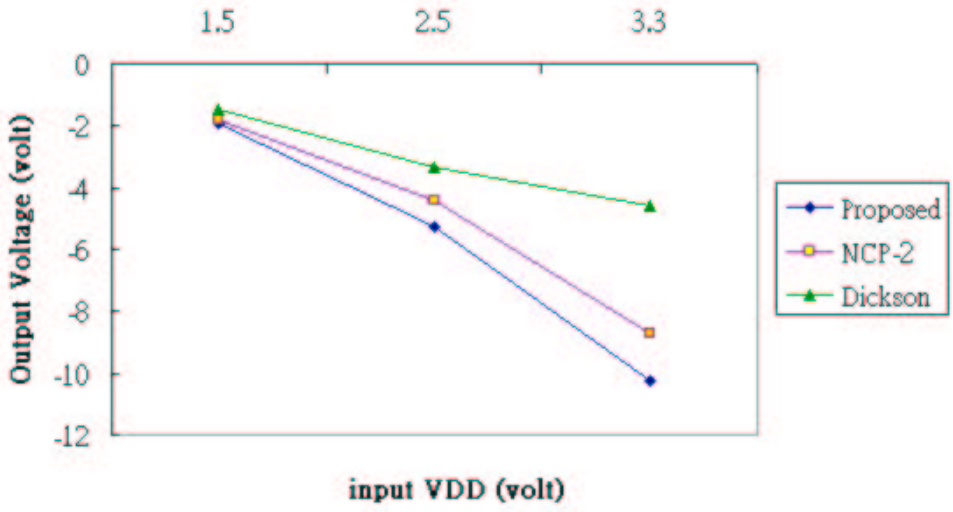

Figure 10: Input VDD vs. output voltage in back bias generator

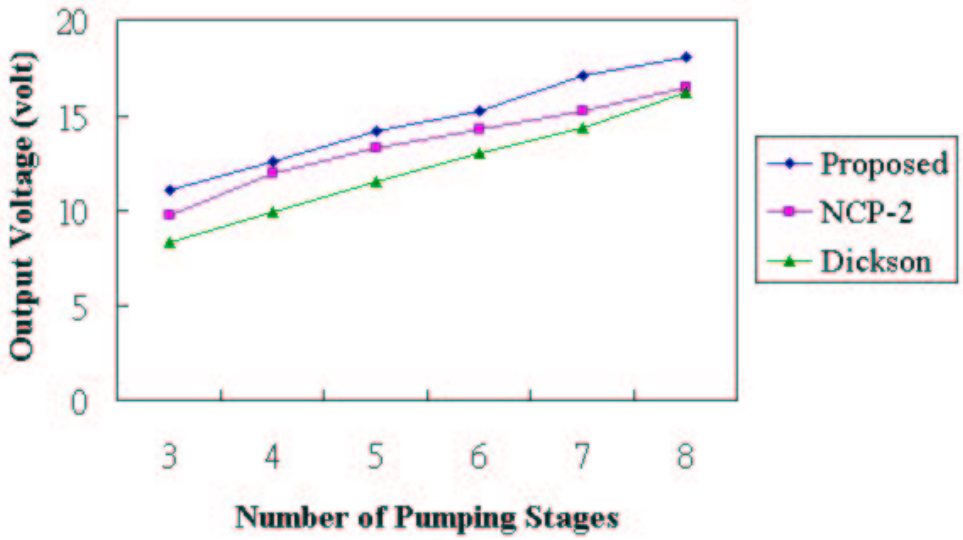

Figure 11: Pumping stages vs. output voltage