第三代行動通訊基地台發射機之時序控制單元設計
Timing Processing Unit Design of 3G BTS Transmitter

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Abstract

In the third generation (3G) WCDMA base station, it's important to control and adjust transmit timing. According to 3GPP FDD standard, downlink timing processing unit (TPU), including cell setup and channel timing control finite state machines (FSM), is implemented. Besides, offset handling of channels is accomplished to manage the transmitting offset in soft handover.

Keywords: 3G, WCDMA, FDD, Timing Processing Unit, Channel Timing Control, FSM, Offset Handling, Soft Handover

1. Introduction

In 3G WCDMA system, downlink (DL) timing control is needed to make sure that channels are transmitted during specified timing position or period. There are two kinds of channels to be conveyed, common channels (CCH) and dedicated channels (DCH). The former broadcast some system information to handsets, like synchronization with the base station. The latter provides different rates of data services, like voice transmission on dedicated users.

After the system power turns on, cell setup and following channel-on procedures should be started. According offsets assigned by upper protocols, it's necessary to consider correct aligned timing. Figure 1 displays timing relation of downlink physical channels[1]. In the proposed system, field programmable grid array (FPGA) is used to accomplish this timing processing unit (TPU).

2. Cell Setup Timing Processing

Cell setup timing control is done via a *T_cell* parameter, which defines the timing delay between cell system frame number counter (SFN) and node B frame number counter (BFN). When a cell is turned on, its timing counter should be delayed *T_cell* relative to node B timing counter to distinguish with other cells in the same node B.

Figure 2 shows the cell setup finite state machine. After the cell is ordered to be setup in next frame, the state will be changed to *zero t_cell state* or *wait boundary state* based on whether T_cell is zero or not. If T_cell is zero, it will enter *complete state* as node B frame boundary comes. That means the cell's timing is the same as the one of node B. If T_cell is not zero, it won't be *complete state* until T_cell delay is achieved. So the starting point of cell will fall behind the one of node B. As the cell is turned off any moment, it must return to *reset state*.

3. Common Channel (CCH) Timing Processing

3.1. Generic CCH Timing FSM

Common pilot channel (CPICH) is a downlink physical channel carrying a pre-defined bit/symbol sequence, shown in Figure 3. It's not necessary to do any control on CPICH because of its continued transmission.

Primary common control physical channel (P-CCPCH) shown in Figure 4, secondary common control physical channel (S-CCPCH) shown in Figure 5 and paging indicator channel (PICH) shown in Figure 6 have their individual channel offsets. So the timing FSM is somehow a little complicated. Before every cell frame boundary, channel offset of next frame should be specified.

The FSM is shown in Figure 7. After the channel offset is processed, *transmission state* is

entered and stayed until reaching *wait boundary state* to check the channel offset and on/off of next frame. There are some chips counting from the frame's end to enter *wait boundary state*.

If the channel is keep transmitting in next frame, the channel offset must be count again in *offset count state*. Then *transmission state* is re-entered. If the channel will be off in next frame, however, some data of previous fame should be delivered completely. The data transmission will exceed the frame boundary because of its offset happened earlier. *Remainder count state*, used to handle this kind of condition, keep on transmitting data until offset counting is over. Naturally, if there is zero offset in the channel, it will be easier to end the channel by going to *channel off state* only and waiting for another channel-on order.

Figure 8 is the flow diagram to show the state transition in time axis.

3.2. SCH and AICH Timing FSM

Synchronization channel (SCH) shown in Figure 9 is a downlink signal for cell search, whose transmission covers every first 256 chips of a slot so P-CCPCH that carries SFN is off during this period. Its FSM is shown in Figure 10. In *on state*, synchronization code generator provides both primary and secondary synchronization codes to let handset find out the burst of every slot.

The Acquisition Indicator channel (AICH) shown in Figure 11 is a fixed rate physical channel to carry Acquisition Indicators (AI), whose FSM is shown in Figure 12. Base station receives preamble signals from handsets via physical random access channel (PRACH). The acquisition indicator is determined and should be delivered three slots after corresponding preamble. Therefore, some enable signals for interface and symbol loading are generated at proper timing.

4. Dedicated Channel (DCH) Timing Processing

The downlink physical channel (DPCH) can be seen as a time multiplex of a downlink dedicated physical data channel (DPDCH) and a downlink physical control channel (DPCCH). Figure 13 shows the frame structure of the downlink DPCH. Five fields are needed in a slot, as data1, transmit power control (TPC), transport format combination indicator (TFCI), data2 and pilot. They may have different gain, respectively. Thus, shown in Figure 14, states of five fields will be entered in turn. Before next slot, gains of five fields in a slot must be known.

Five counters of slot fields are also implemented to compute the chip time processed. Different slot formats may have different data rate, field duration and gain, read from DSP and maintained in FPGA hardware.

5. Summary

Timing control of the cell and channels in the base station is sometimes confusing. It will be clear to implement by using several FSMs. Channel offsets and relative timing can be fully controlled to meet 3GPP spec.

Timing accuracy is verified via simulation and physical probing measurement. Different cases are processed to test all kinds of state transitions. Co-verification with DSP is also completed to make sure the function of whole BTS system.

6. Reference

[1] 3GPP TS 25.211: "Physical channel and mapping of transport channels onto physical channels (FDD)."

[2] 3GPP TS 25.213: "Spreading and modulation (FDD)."

[3] 3GPP TS 25.104: "BS radio transmission and reception (FDD)."

[4] Lilja, H.; Mattila, H. "WCDMA uplink modulation scheme evolution and transmitter implementation", Vehicular Technology Conference, 1999. VTC 1999 - Fall. IEEE VTS 50th , Volume: 2 , 1999

[5] Chia, S.T.S.; Lee, W.C.Y. "A synchronized radio system without stable clock sources", IEEE Personal Communications , Volume: 8 Issue: 2 , April 2001 Page(s): 45 -5

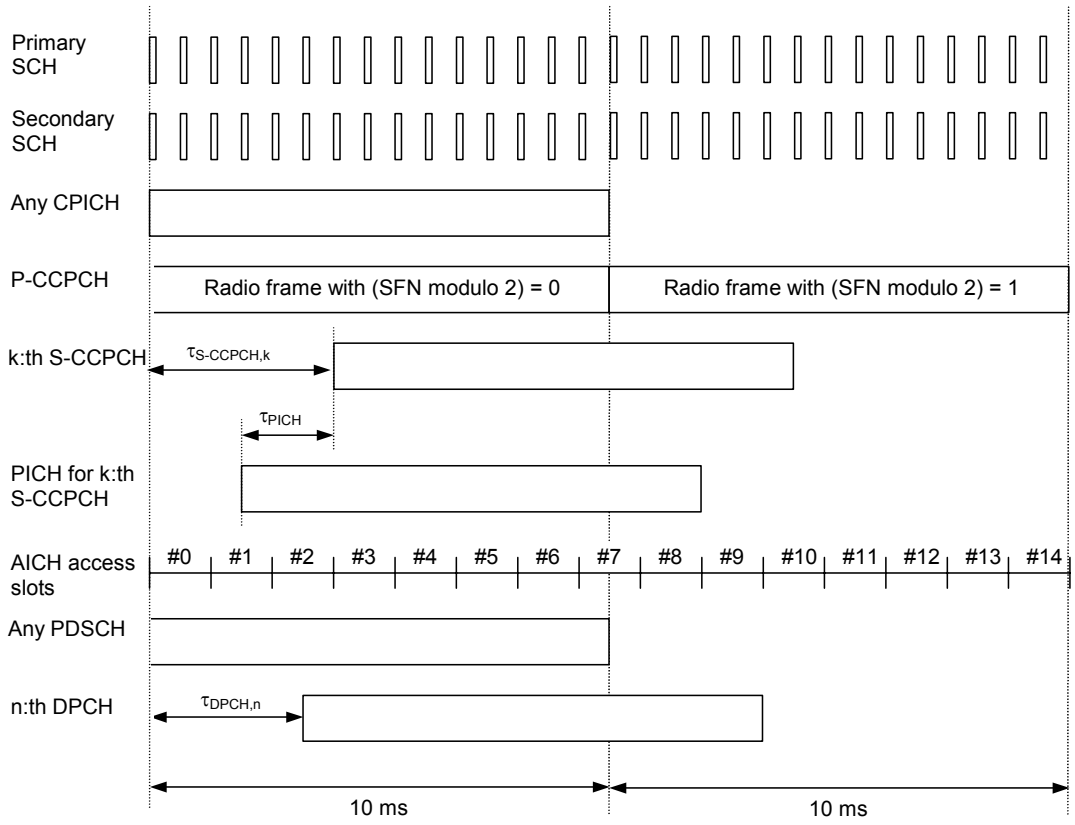

Figure 1, timing relation of downlink physical channels

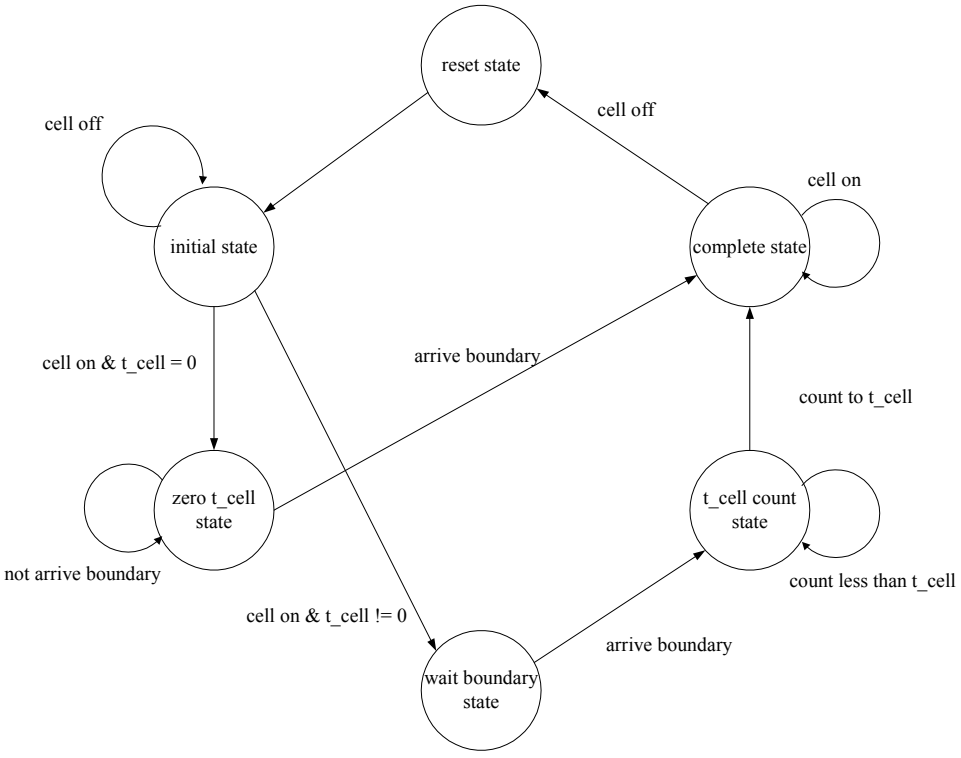

Figure 2, cell setup timing finite state machine

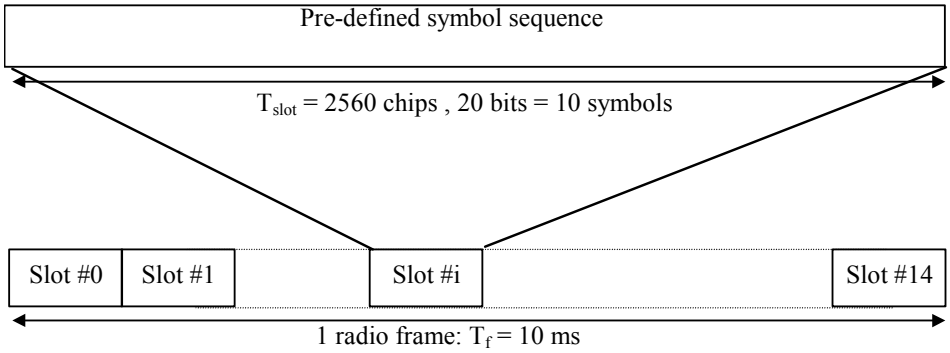

Figure 3, frame structure for common pilot channel

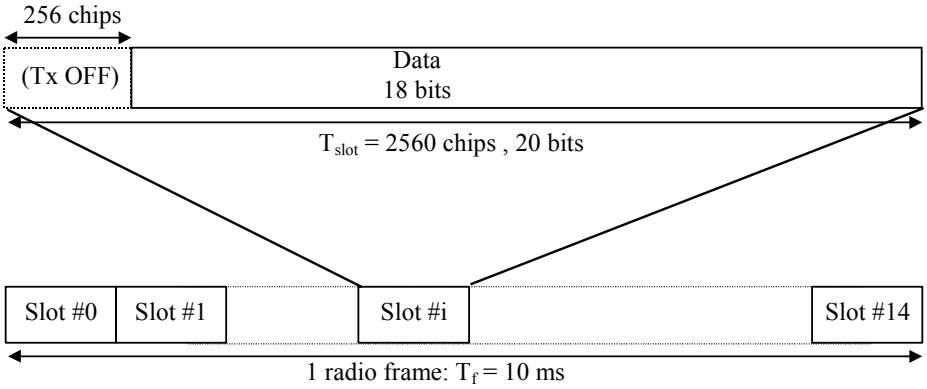

Figure 4, frame structure for primary common control physical channel

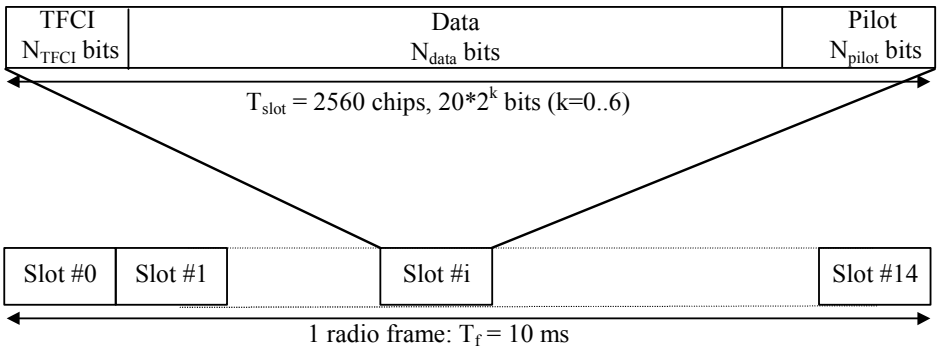

Figure 5, frame structure for secondary common control physical channel

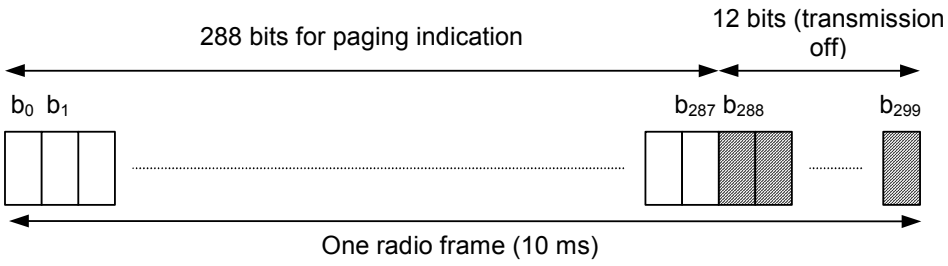

Figure 6, structure of paging indicator channel

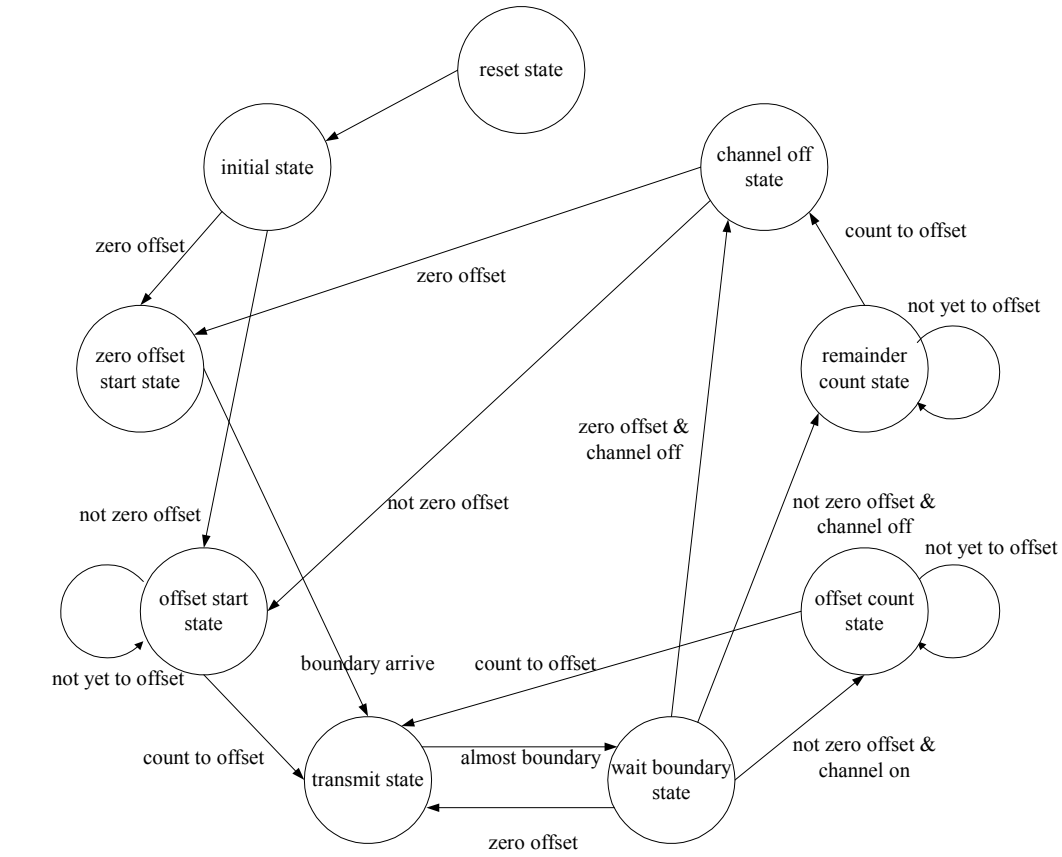

Figure 7, generic CCH timing finite state machine

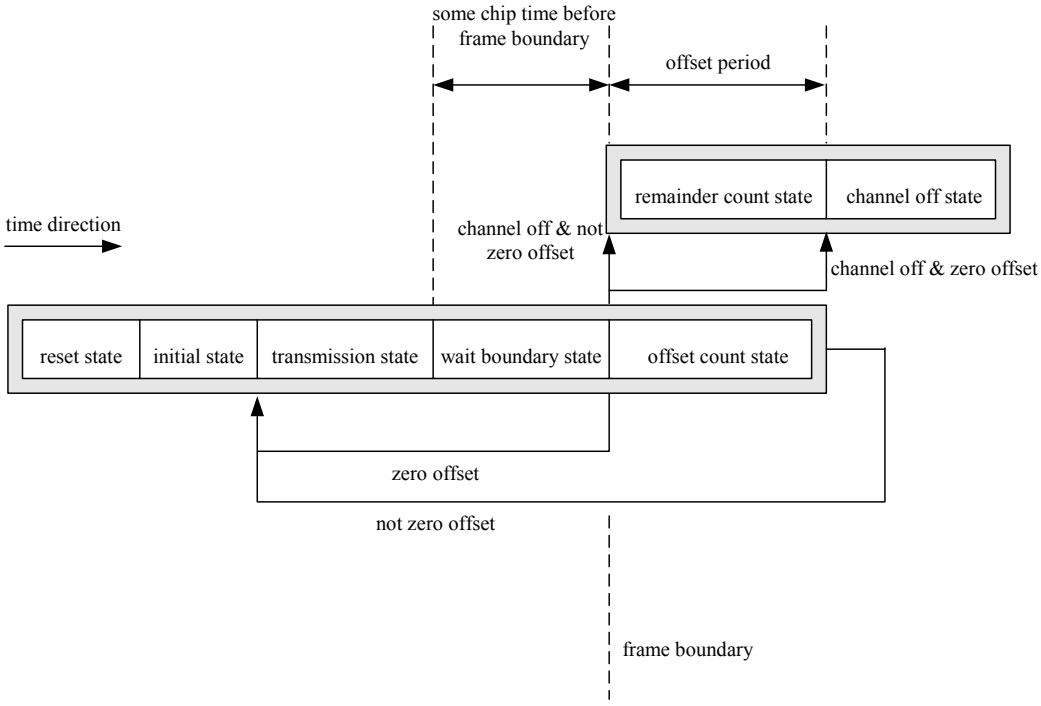

Figure 8, generic CCH timing flow

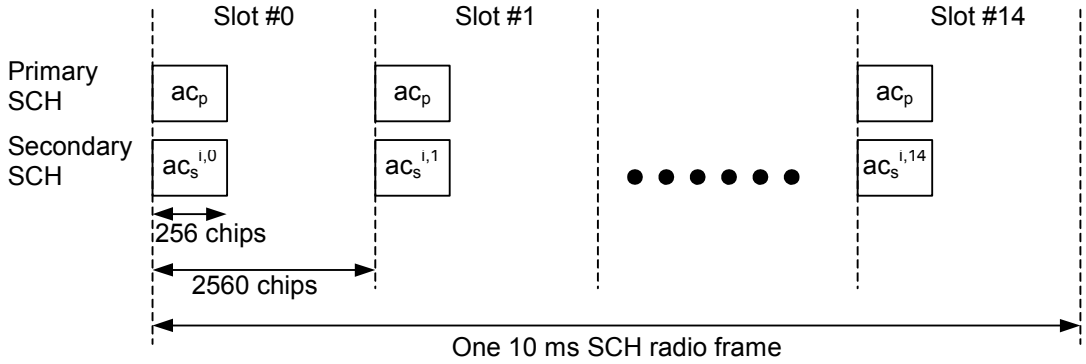

Figure 9, structure of synchronization channel

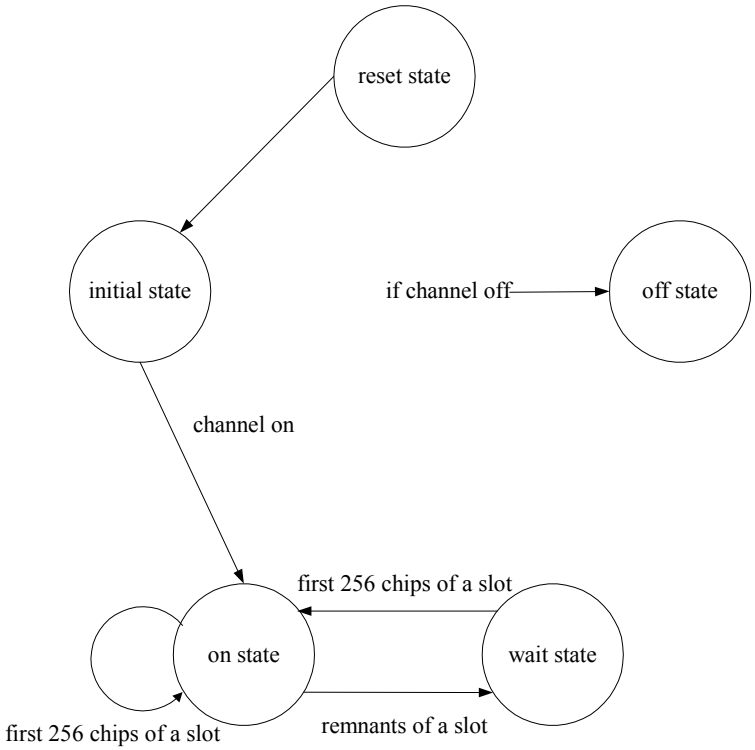

Figure 10, SCH timing finite state machine

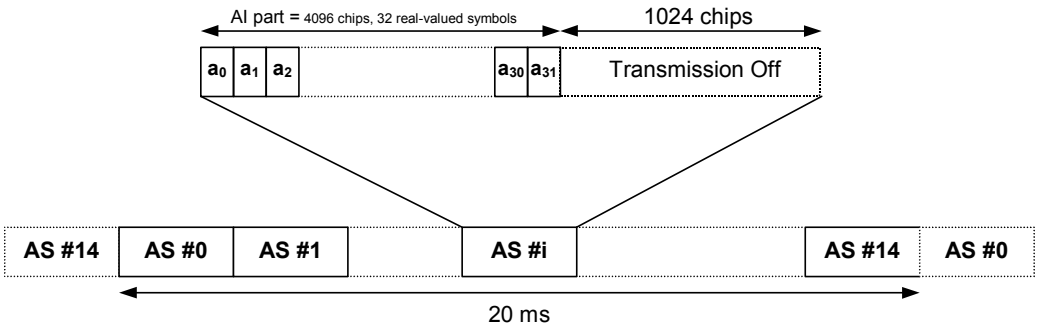

Figure 11, structure of acquisition indicator channel

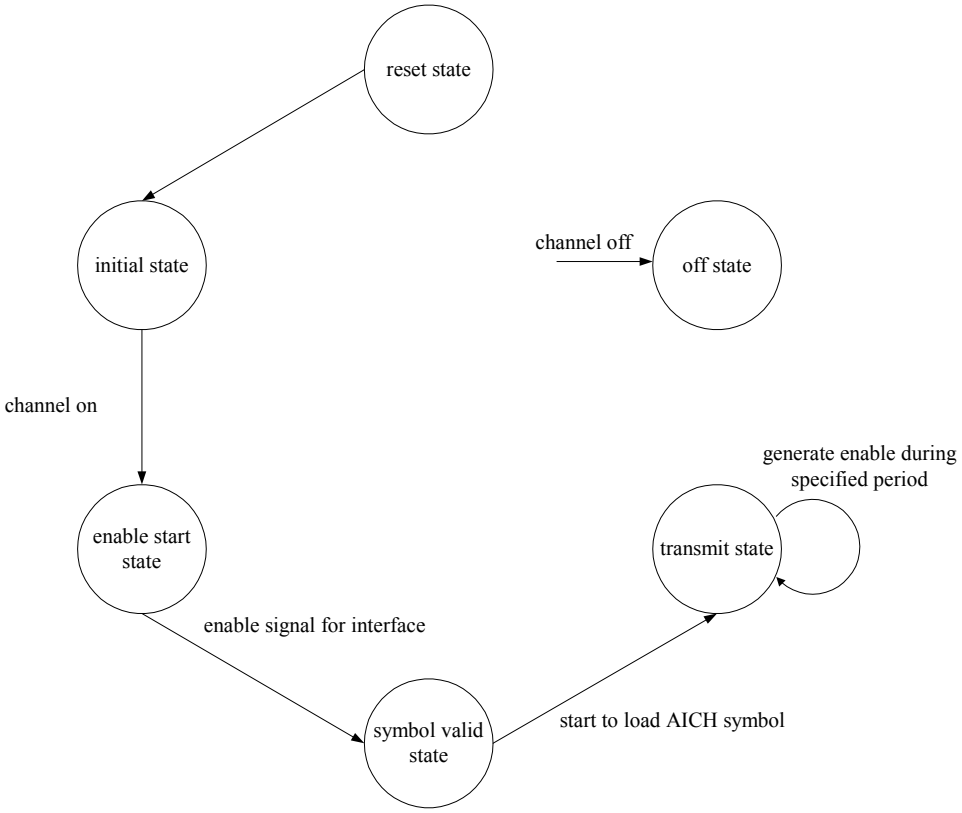

Figure 12, AICH timing finite state machine

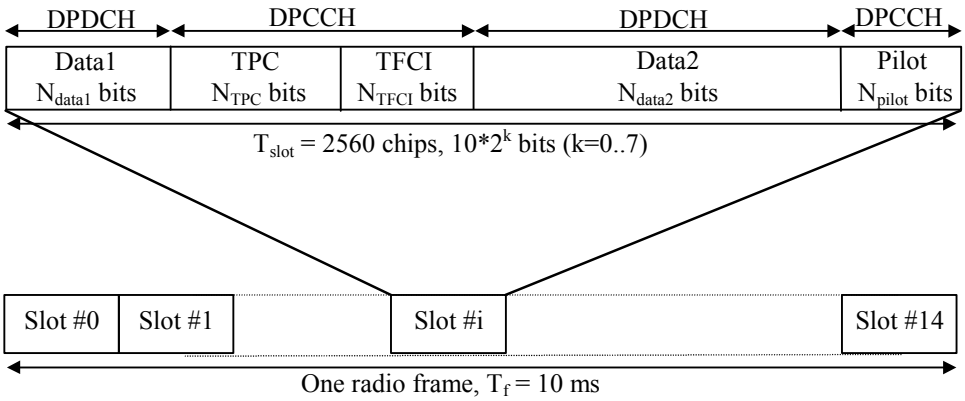

Figure 13, frame structure for DPCH

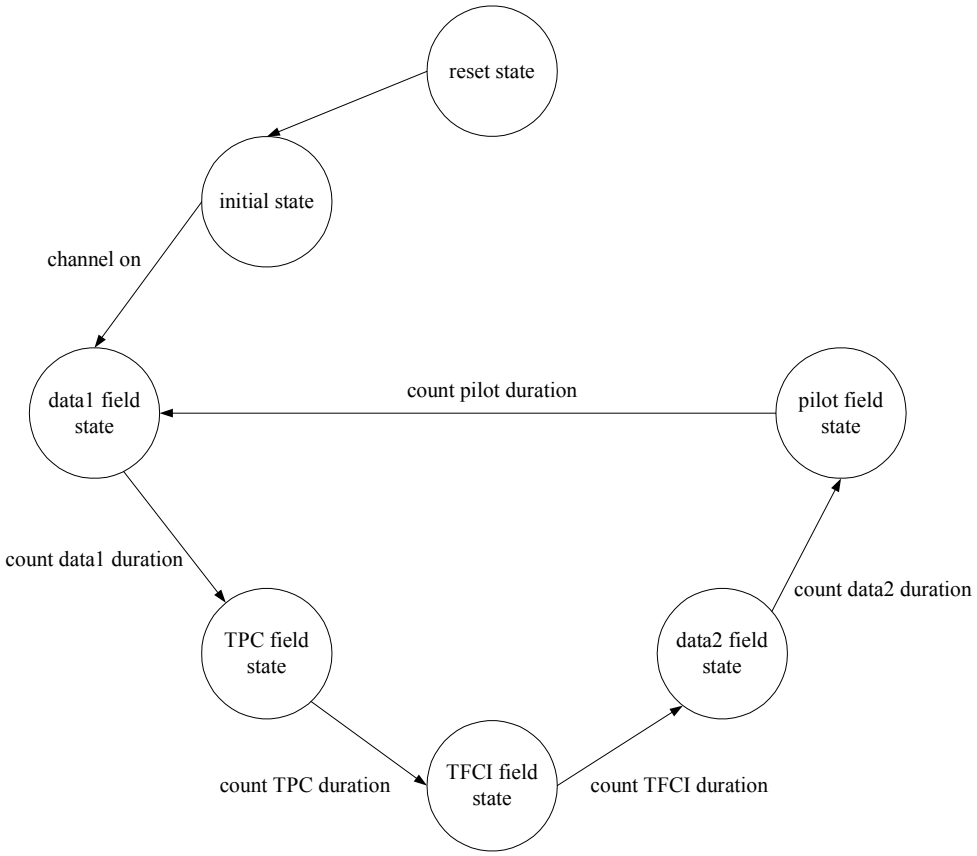

Figure 14, dedicated physical channel timing finite state machine