Design and Implementation of a High Efficiency Digitally Controlled DC-DC Boost Converter

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***Abstract*—A digitally controlled dc-dc boost converter operating in CCM mode is implemented and presented in this thesis. The digital controller of the converter system is realized with an 8-bit (G6053) microcontroller configured as digital compensator to perform compensation on the voltage control loop of the system. The minimum resolution requirement for A/D conversion is discussed to meet the condition of tight output voltage regulation. Also, the analog module feature of G6053 microcontroller is configured to produce PWM signal instead DPWM. It is observed that the digitally controlled converter system achieves the main objectives of power conversion – regulation and high efficiency. The prototype converter has 91% efficiency with a 200mV ripple voltage performance. Additionally, the converter system operates in a wider input voltage range of operation.**

***Index Terms*—digitally controlled, boost converter, 8-bit microcontroller**

I. Introduction

DIGITAL control of switching dc-dc power supply provides a better solution than the analog control as the cost of most digital circuits has been reduced significantly recently. Compared with analog circuit control, digital controllers provide a quite number of advantages, including flexibility, less susceptible to environmental noise, fewer passive components, portability and programmability. Fig.1 shows a diagram of a typical digitally controlled switching dc-dc converter. It consists of ADC (Analog-to-Digital converter), processing unit, and a digital pulse width modulation (DPWM). The processing unit acts as a regulator of the controller that implements control law. In this architecture fast implementation of a discrete-time control law is necessary in order to achieve dynamic characteristics comparable with analog PWM controllers.

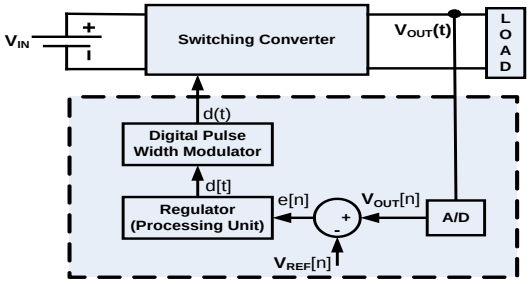

Fig.1. Typical block diagram of a digitally controlled switching converter

II. The Proposed Architecture

Fig.2 shows the diagram of the digitally controlled voltage mode dc-dc boost converter prototype operating in CCM.

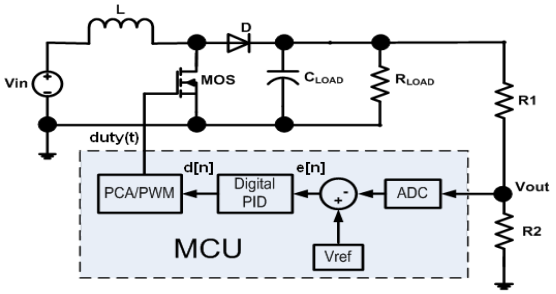

Fig.2. Digital controlled dc-dc switching boost converter prototype

The prototype utilized an 8-bit microcontroller (G6053) from INNO-TECH CO., as its digital controller. The purpose of power feedback system is regulating the output voltage to match a precise, stable voltage reference over a range of input voltage and load current. From Fig.2, we can see that a digital controlled converter contains three major components/modules that are totally not available in most analog controlled converter, which components are ADC, Digital PID and PCA/PWM. In the voltage mode boost converter, the output voltage is sampled by an analog-to-digital converter and

compared to the reference then produced digital error signal e[n]. The error signal is passed to the digital compensator which is to take the e[n] and previous e[n-1] samples of the error signal and compute the new value of d[n]. The output of digital PID is the input to the programmable counter array (PCA) configured as PWM generator, which in turn produces the duty ratio signal to control the switching power transistors. The operation iterates until the output voltage is approaching to the reference voltage.

A. ADC (analog-to-digital converter)

In the case of dc-dc regulated power supply, its main function is to quantize the regulated signal (feedback) into a digital word. The process of analog-to-digital conversion often involves two important actions which are extremely essential to system performance and control design. The ADC module of G6053 microcontroller utilized successive approximation ADC type architecture which is using binary search algorithm continues to repeat the searching process until all N bits are determined. Literature [2] employ digital controller (MCU) with successive approximation A/D converter architecture for its ADC operation. Generally, the binary search algorithm divides the search space in two each clock cycle, and the desired data can be sought in N steps for a set of sorted data of size 2^N. Thus, the implementation of successive approximation ADC requires N clock cycles to complete an N-bit conversion.

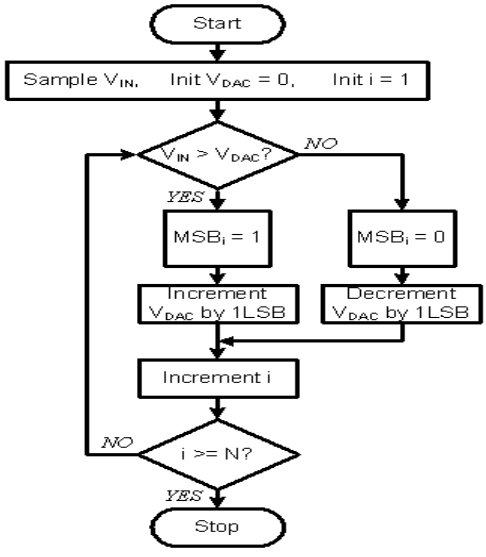

Fig.3 Flow graph for SAR approach

Fig.3 shows the flow graph of successive approximation approach pattern from binary search algorithm. To ensure the ADC maintains the accuracy of the output signal the ADC clock source is configured to generate 77 kHz as its operating sampling frequency. For this sampling frequency the conversion time of the on-chip ADC is fixed at 13μs.

The ADC module takes as its input signal a portion of the output voltage through a feedback network, which is composed of two resistors connected in series. Literature [3], clearly pointed out that equation (1), with a given ΔV_O the minimum requirement of ADC is 10-bit, which is exactly the featured resolution of G6053 microcontroller.

$$n_{a/d} = \text{int}\left[\log_2 \frac{V_{MAX_{a/d}}}{V_{REF}} \cdot \frac{V_O}{\Delta V_O} \right] \qquad (1)$$

As a result, for a voltage level set to the maximum voltage requirement of the ADC and with a 10-bit resolution or 1024 discrete levels, the ADC can generate a base resolution of 3.3/1024 or 3.2mV between levels. However, for this prototype the on-chip ADC module takes half of the minimum voltage requirement as its input voltage, which is then compared to a numerical voltage reference to produce an error signal. For the given reference voltage, which corresponds to 1.65V, the voltage divider network produces an output voltage resolution of 48/1024 or 46.8mV between levels.

B. Digital PID Controller

The difference between the feedback signal and numerical voltage reference serves as the controlling signal for driving the duty cycle of the converter. The duty cycle was then calculated using a discrete proportional-integral-derivative (PID) controller. Fig.4 illustrates the typical PID structure of a digital compensator.

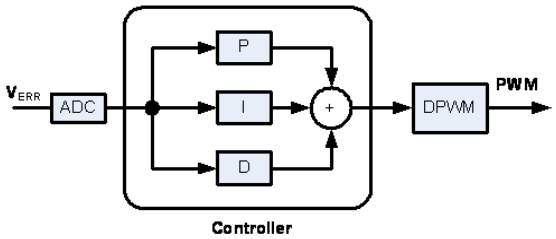

Fig.4 Diagram of digital PID compensator

The continuous time transfer function of a PID controller is given as:

$$G_C(s) = K_P + \frac{K_I}{s} + K_D s \qquad (2)$$

The transfer function in equation (2) is converted to a difference equation for digital implementation using bilinear or backward transformation method. Once it has been converted to difference equation it is now suitable for computation by a computer. The difference equation of equation (3) can take the form of:

$$d(k) = K_{PA}e(k) + K_{IA}T\sum_j e(j) + \frac{K_{DA}}{T}\left[e(k) - e(k-1)\right] \quad (3)$$

Equation (3) can be further written as:

$$d(k) = K_P e(k) + K_I \sum_j e(j) + K_D\left[e(k) - e(k-1)\right] \quad (4)$$

However, due to the presence of set-point in the derivative term, which will cause an unwanted change in duty cycle due to disturbances, equation (4) is modified to:

$$d(k) = K_P e(k) + K_I \sum_j e(j) + K_D\left[PV(k) - PV(k-1)\right] \quad (5)$$

Now here, K_P, K_I, and K_D are digital proportional gain, digital integral gain and digital derivative gain, respectively. The variable *d(k)* is the computed duty cycle for the k^{th} sample of the output voltage. The variable T is the sampling period and *e(k)* is the error signal between the measured output voltage (process value) and the desired output value (set point value). Furthermore, the gain constants of each term of the PID controller are properly chosen to ensure the prevention of the output voltage from oscillation and guarantee the optimal control of the system (system's stability). Finally, for this prototype K_P *= 1/16*, K_I *= 1/32* and K_D *= 1/64* are selected.

C. PWM Using Programmable Counter Array

Most systems relating to power converter utilize pulse width modulation technique in regulating the output voltage. As for digital controlled power converters the technique of digital pulse width modulation is the most widely implemented method in realizing voltage regulation. The implementation of DPWM in generating discrete duty cycles is never opted and realized due to complexities in handling quantization effects as well as frequency limitations of the G6053 microcontroller. Instead, it utilized the analog module in the microcontroller which is the programmable counter array (PCA) configured as PWM generator. The PWM signal of the microcontroller is 8-bit resolution. Fig.5 shows the internal architecture of the PCA register using module 1 (n = 1) of the G6053 microcontroller.

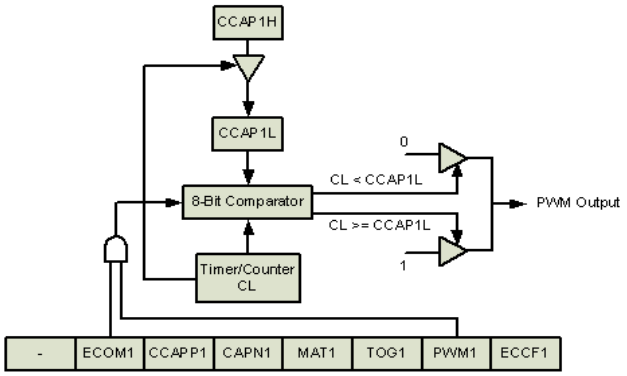

Fig.5 Use of PCA to produce PWM output

The PCA register is configured into PWM mode by setting ECOM1 and PWM1 to logical bit 1. The ECOM1 and PWM1 registers are located in CCAPM1 special function register or SFR. Fig.6 shows the comparison between the low byte CL of the PCA Timer/Counter and the low byte CCAP1L. The high byte is utilized to automatically reload the CCAP1L every time it goes to zero. It goes to zero when CL has incremented up to its value. The CCAP1H register, on the other hand, serves as a marker fixing the on (e.g. 3.3V) off (0V) ratio of the PWM signal. Since the PWM is 8-bit, cycle time of the PWM is 256 PCA time clock cycles. In addition, the 8-bit PWM controls the output voltage to a resolution of 0.390 percent (%) or written as:

$$\mathrm{Re}\,solution_{PWM} = \frac{1}{2^N} \times 100\% \quad N = number\ of\ bits \quad (6)$$

In one PWM cycle CL increases from zero up

towards the value of CCAP1L, which is automatically loaded from CCAP1H. During this period, when CL < CCAP1L, the PWM output is logic 0 (0V). When CL = CCAP1L it momentarily goes to zero but is immediately reloaded from the contents of CCAP1H. During this time CL continues to increase for the period CL >= CCAP1L and the PWM output goes to logic 1 (3.3V). The effect of this operation is illustrated in Fig.6.

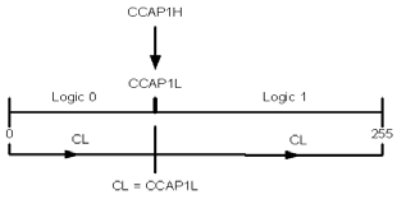

Fig.6 Effect on output logic level as CL increases from 0 to 255.

III. Design Example And Simulation Result

To demonstrate closed-loop operation, the controller is used with boost converter shown in Fig.7. Furthermore, using the state space averaging model, the small-signal transfer function from the duty cycle (*D*) of the switch to the boost converter output (Vo) can be derived below:

$$G_{vd} = \frac{\hat{V}o}{\hat{d}} = \frac{V_{IN}}{(1-D)^2} \times \frac{-\frac{1}{R_L C} z + (1-D)^2}{z^2 + \frac{1}{R_L C} z + \frac{(1-D)^2}{LC}} \qquad (7)$$

The allowable input voltage range for each operating load condition is between 8V – 20Vdc. In Fig.2, the desired output voltage is 24Vdc and is desired to keep constant under all operating conditions and disturbances, such as input voltage and load variations. The operating switching frequency is equal to a software selectable value of 46 kHz. It is generated internally by an 8-bit microcontroller, which has a crystal-oscillator based clock frequency of 12MHz. Further, the inductance and capacitance of this prototype were 1mH and 100uF, respectively. The 1mH inductance was chosen to be greater than the minimum required value to ensure the current is operating in continuous mode.

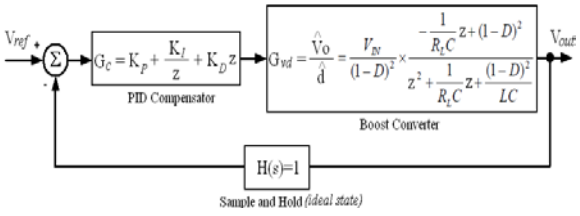

Fig.7 Model of closed-loop control system

By the employment of MATLAB for the frequency-domain simulation, Bode plot of the control to output transfer function is shown in Fig.8. From the result, the close-loop phase margin is 63.7 deg, which indicates the control loop is stable.

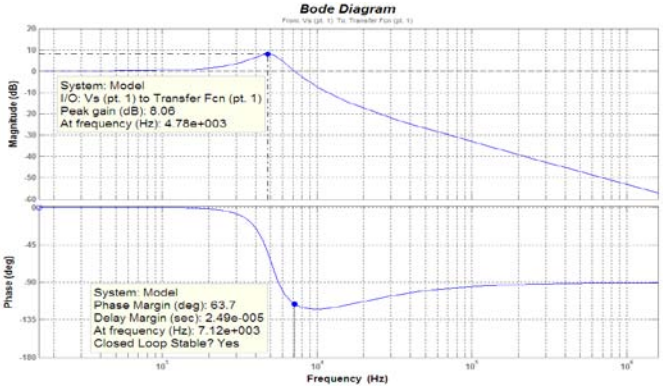

Fig.8 Bode plot of close-loop transfer function

The loop behavior has been carried out with MATLAB/SIMULINK, base on the small-signal model and transfer functions. The model system simulation for the voltage mode controlled boost dc-dc converter operating at the switching frequency of 46kHz. The block diagram of the system and output signal versus time result of boost converter shown in Fig.9 and Fig.10.

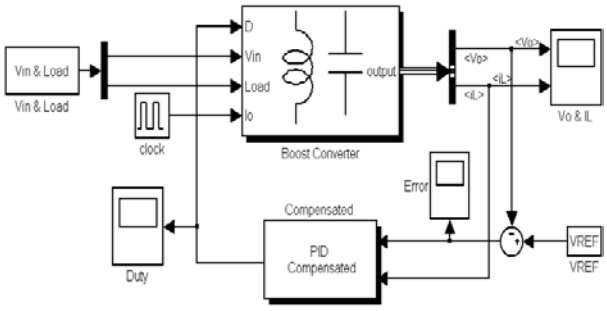

Fig.9 Circuit simulation block diagram using MATLAB/SIMULINK

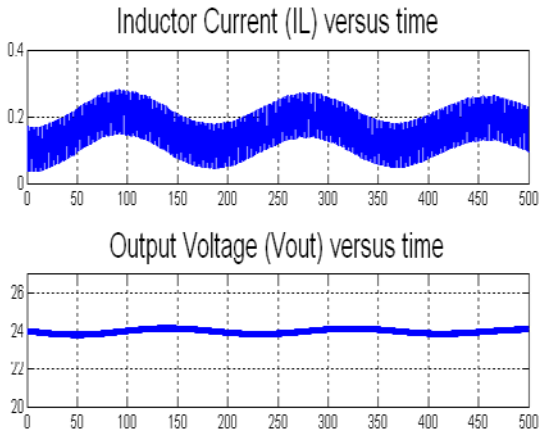

Fig.10 Simulation of Vout and IL versus time

IV. Experimental Results

The PCB layout of the digitally controlled dc-dc boost converter is shown in Fig.11. Here, two knobs are placed in front of the PCB for easier control of the system. The first knob on the left side serves as the tuning apparatus for the feedback resistor in order to get an appropriate voltage level for the ADC input of the microcontroller. Once the tuning of the desired output level is satisfied, it is then replace by a fixed resistor. The second knob on the right side serves as the load resistor selector.

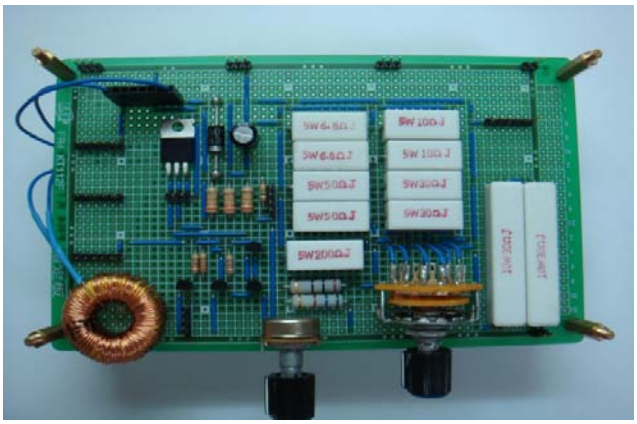

Fig.11 PCB Layout of the prototype circuit

It can be observed from Fig.12 and Fig.13, the measurement result shows the vout=24.2V between line and load transient. The waveform show in the Fig.12 is categorized as follows: output voltage (top), pwm signal (middle) and inductor current (bottom). Under these conditions, the value of the output voltage is unaffected by the disturbances occurred in the load. Moreover, the duty cycle of the pwm signal has displayed an almost constant width value all throughout the transition.

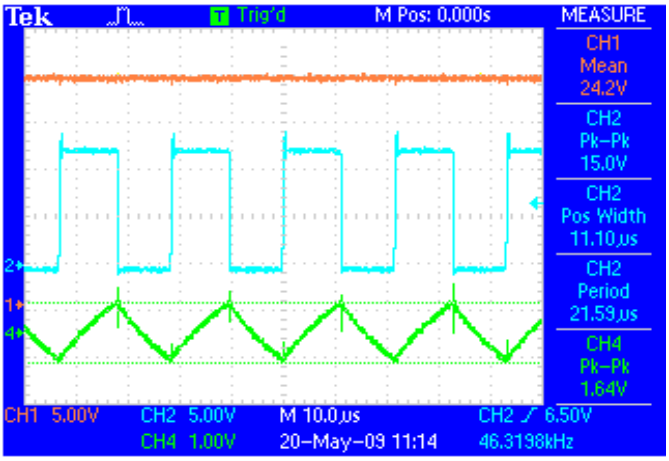

Fig.12 Converter system waveforms for load regulation at R_L = 571Ω to R_L = 115Ω transition

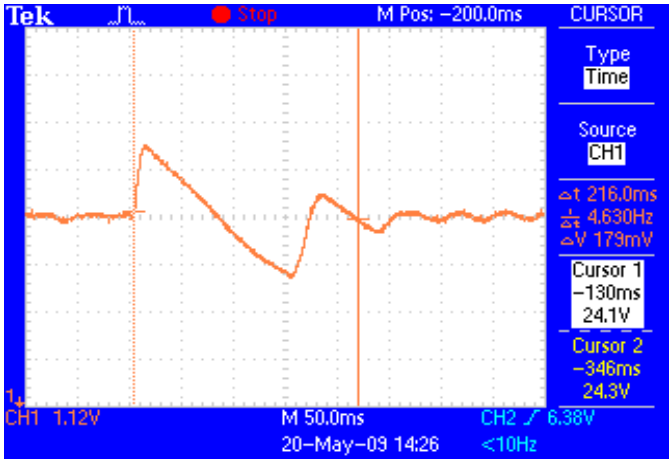

Fig.13 Transient response at 12V-13V transition

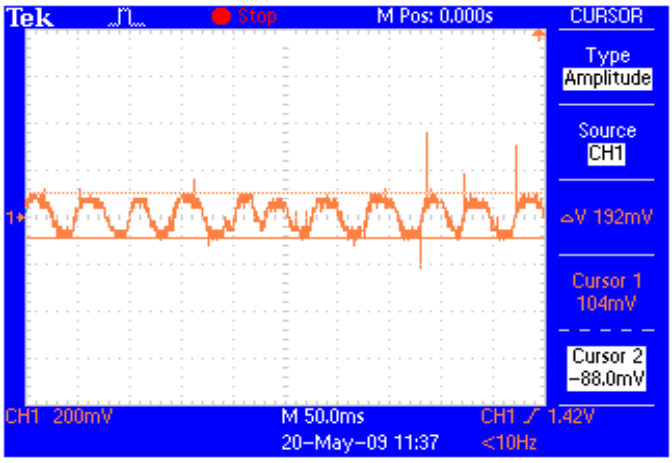

Fig.14 Ripple voltage at R_L = 571Ω

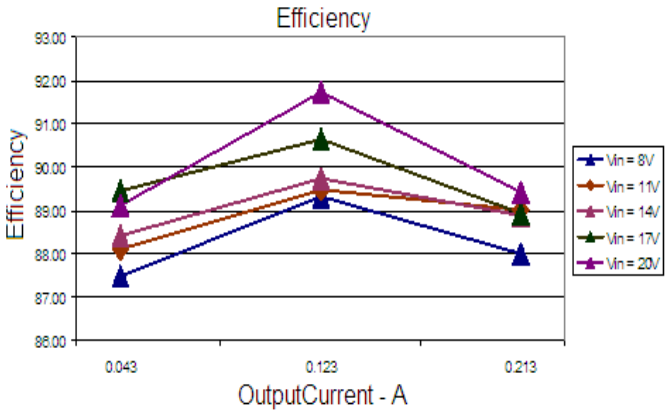

Fig.15 Efficiency of the digitally controlled dc-dc boost converter

V. Summary

The design circuit of the system including G6053 microcontroller voltage is 3.3V, ADC is 10-bit, and allowable input voltage range for each operating load condition is between 8V – 20Vdc. The desired output voltage is 24Vdc and is desired to keep constant under all operating conditions. The operating switching frequency is 46 kHz. Fig.14 and Fig.15 shows the prototype converter has 91% efficiency with a 200mV ripple voltage performance.

VI. Conclusion

In this thesis, the practical design and implementation of a simple digitally controlled dc-dc switching boost converter operating in continuous current mode (CCM) is presented. As for keeping the boost converter invulnerable to switching noise, the pulse width modulation technique (PWM) is being utilized due to its fixed frequency behavior. In realizing a better performance on the system, the boost converter prototype utilized an 8-bit microcontroller (G6053) from INNO-TECH CO., LTD as the digital controller compensator, which is configured to provide sufficient compensational parameters to the system. The implementation of the digital compensator is purely based on the concept of proportional-integral-derivative (PID) algorithm. As for the performance of this prototype, the G6053 microcontroller provides a one-chip solution for a voltage mode control switching dc-dc converter.

Acknowledgment

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