Graph-based Wire Planning for Analog Circuits

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***Abstract*—In this paper, we propose the graph-based approach which constructs the electromigration-free wire planning according to the current characteristics of sources and sinks. The objective of this paper is to minimize the total wiring area of the wire planning without electromigration, i.e. enhance the mean time before failure. First, we construct the complete bipartite graph which the weight of each edge is with consideration of distance between each source-sink pair and current capacity for all sources and sinks. Second, we sort the weights of all edges with the ascending order. Third, the edge with the minimal current-distance weight is selected to remove from the complete bipartite graph. Furthermore, we iteratively update the supply current of the current source and the weights of the corresponding edges which are connected to the current source. Finally, the greedy method terminates until the current capacity of all sources are zero. Five benchmark circuits are used to evaluate the proposed algorithm and experimental results show that the proposed approach efficiently gets the better solution and effectively minimizes the wiring area with consideration of electromigration.**

***Index Terms*— Electro migration, space reservation, Wire Planning, Obstacle-avoiding routing, Graph theory.**

I. INTRODUCTION

Automation of analog circuit is getting more and more important. Traditionally, the analog circuit is designed by using the manually because there are huge experiences to produce the analog circuit with the high performance and the better circuit characteristics. Nowadays, some researches focus on the circuit automation [7][8] such as the placement of summitry, parameters determination by mathematical programming, automation wire planning to enhance circuit reliability [9].

A. Previous works about wire planning

Automation of wire planning plays an important role on the circuit reliability. Lienig *et al.* introduced the physical design flow which integrates current-driven planning and verification and presented a concept to assign the large current value to the short path with consideration of electromigration. [8]. Jerke *et al.* presented the post-routed approach to modify the critical layout structures to increase the reliability and reduce the number of violations [3]. Lienig et al. proposed a new approach, which effectively determines all wires width in the given terminals [14]. Furthermore, their approach is verified by using a real world analog design. Adler et al. presented a single layer router, which satisfies the current constraints and the maximum current density for all interconnect [1]. Adler *et al.* proposed a new greedy-based approach, which determines the wire width for a multi-terminal net with consideration of the obstacles, to solve the current-driven routing problem [2]. With consideration of the obstacles, their approach can find the proper routing path according to the wire width and the available routing space between the adjacent obstacles. Lienig *et al.* provided two approaches to handle the analog multiple terminals net while satisfying the Kirchoff's current law [14]. Besides, they discussed the concept of the over-sizing for the arbitrary polygon. Lienig *et al*. proposed an analog router, which handle non-rectangular obstacles with the non-Manhattan-based routing, for the current-driven routing [15][16]. Yan *et al.* propose the greedy-based method to minimize the total wiring area to satisfy Kirchoff's current law without the obstacles [18]. Most of them can not obtain the optimal current-driven wire planning.

B. Previous works about obstacle-avoiding routing

Many routing algorithms are presented to minimize the total wirelength with obstacles. Chiang *et al.* [6] proposed the octilinear Steiner tree algorithm by using the edge-conversion and

Steiner-sliding approaches. Ho *et al.* [10] provided the X-arch Steiner tree algorithm to use the Delaunay triangulation to cluster terminals and sort total length of each three-terminal to generate the optimal connection. Shen *et al*. [17] proposed a graph-based method which first constructs a graph by the terminals and obstacles, finds the minimal spanning tree from the connection graph and construct the rectilinear Steiner tree. However, most of them deal with the digital circuit without consideration of the circuit characteristics of analogy circuits.

C. Contribution of our works

The contributions of this work are as follows. First, to avoid the electormigration of the circuit, the greedy-based approach, which formulates the problem into the graph model, is used to automatically determine the feasible connections between sources and targets with the proper wire width. Second, to avoid the interference between the obstacle and wires, the space reservation [5][11] is utilized for all obstacles. Third, the proposed method, which computes the obstacle-avoiding length by using the push_line method, efficiently determines the routing path to reduce the total wiring area with the current capacities of all sources and sinks.

D. Outline of the proposed work

The rest of the paper is as follows. Section II describes the terminology and the problem formulations. The Section III discusses the proposed algorithm with an example in detail. The experimental results and conclusions are attached in Sections IV and V, respectively.

II. PRELIMINARY

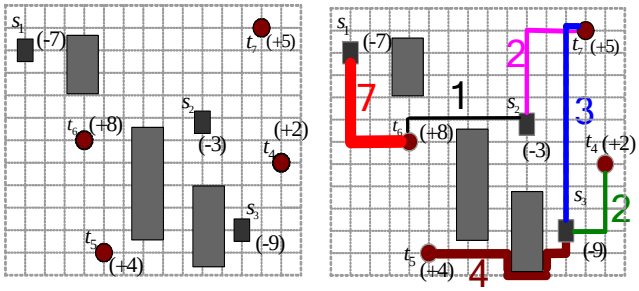
In the section, we first discuss the terminology and then define the problem formulation. In the paper, the Manhattan-architecture which supports the vertical and horizontal segments for the routing is applied to connect for the sources and sinks with consideration of the current capacity.

A. Terminology

First, the wirelngth with consideration of obstacles is discussed. With consideration of the obstacle penalty, the wire length due to the obstacles [12][17] is involved in the cost function. For each connection between source $s_i = (x_i, y_i)$ and target $t_j = (x_j, y_j)$, the obstacle-avoiding Manhattan length is estimated as follows,

$$d(i,j) = |x_i - x_j| + |y_i - y_j| + \min(len_u(i,j), len_l(i,j)) \quad (1)$$

where $len_u(i,j)$ and $len_l(i,j)$ denote the additional obstacle-avoiding wire lengths of the upper-L and low-L routing paths, respectively.



(a) Original circuit (b) results

Figure 1. Illustration of wire planning.

Second, we illustrate the formula to compute the total wiring area. The wiring area of the current-driven wire planning is defined by,

$$A = \sum_{i,j} \alpha \times c(i,j) \times d(i,j) \quad (2)$$

where A is the total wiring area of the certain wire planning. $c(i,j)$ and $d(i,j)$ are the capacity and distance for source i and sink j

For Figure 1(a), the wiring area of the wire planning obtained by the heuristic algorithm proposed by [18]. In the paper, the graph-based method is proposed to solve the problem of wiring planning with the obstacles. The additional wirelength due to the obstacles could be taken into

account by using our proposed method. With the obstacles, the total the wiring area of current-driven M-arch wire planning by the

$$7\times7+1\times7+2\times7+3\times10+2\times5+4\times10=150 \quad (3)$$

Above discussion show the formula to compute the total wiring area for the M-arch wire planning.

B. Problem Definition

For the copper or aluminum interconnect the electromigration result in open or short if the wire width is not sufficient. To increase the reliability of the interconnect with the minimization of wiring area, we should assign the minimal wire width according to the current density among the sources and targets. We propose the current-driven routing algorithm which automatically determines the wire widths for all wires with obstacles. Therefore, we define the problem as follows,

Given a net N containing a set of sources $S=\{s_1,s_2,...,s_n\}$ and a set of targets $T=\{t_1,t_2,...,t_m\}$ with their corresponding root-mean-square current values $\{O_1,O_2,...,O_n\}$ and $\{I_1,I_2,...,\mathrm{I}_m\}$, respectively. Besides, there is a set of obstacles $B=\{b_1,b_2,...,b_k\}$ in the analog circuit. The objective is to construct an X-arch wire planning with minimal wiring area with consideration of the obstacles and Krichhoff's current laws [3][4].

III. The Graph-based Wire Planning

In this section, the graph-based greedy method is proposed to perform the wire planning to minimize the total wiring area. Four steps of the algorithm are first discussed and an example is used to illustrate the operation.

A. Description of greedy graph-based method

First, we construct the bipartite graph according to the relationship of all sources and all sinks. The noise idea which is inversely proportional to the distance between adjacent wires is proposed in [19][20]. To avoid the interference between the obstacle and interconnections, we reserve the dead-space along the obstacle.

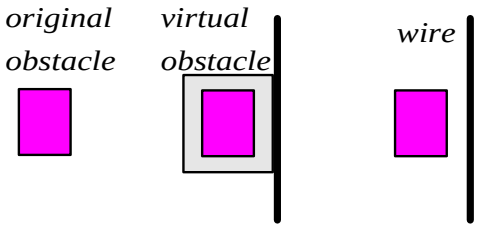


Figure 2. Avoid the interference

The weights of all edges in the complete bipartite graph are assigned by the formula,

$$w(i,j)=\alpha\times d(i,j) \quad (4)$$

where $d(i,j)$ are the distance for source i and sink j, respectively. Besides, α is the ratio between the current capacity and the assigned wire width. To reduce the total wiring area with consideration of electromigration, the proper wire width is determined according to the information of the bipartite graph.

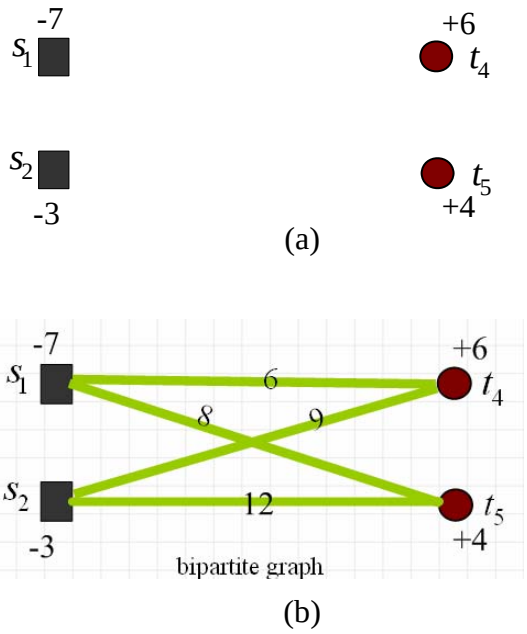
Second, we sort the weights of all edges with the ascending order. We first deal with the edge with minimization product of distance and current capacity. It means that the edge with the current minimal weight is selected to remove from the complete bipartite graph.

Third, we update the supply current of the current source and the weights of the corresponding edges which are connected to the current source. Of course, we should check if the total current capacities of all sources are equal to the total current of all sinks.

Finally, the greedy method terminates until the current capacity of all sources are zero. In other words, the total driving current of all sources is equal to the total sinking current of all sinks.

B. Example to illustrate the operation

We take the following example to illustrate the concept of the graph-based method. Figure 3(a) and (b) denote the original circuit with two sources (black squares) and two sinks (dotted circles) and the complete bipartite graph. Figure 3(c) is the results when we select the edge with 6 current values. The current value of source 1 is update to "-1" (i.e. -7+6). The corresponding results are shown in Figure 3(d) after removing a edge for the complete bipartite graph. Figure 3(e) and (f) are the results when we iterative update the current for the sources and remove the other edge for the complete bipartite graph. Finally, we observe the total currents of the source are all assigned to all sinks by the graph-based method, see Figure 3(g) and (h).



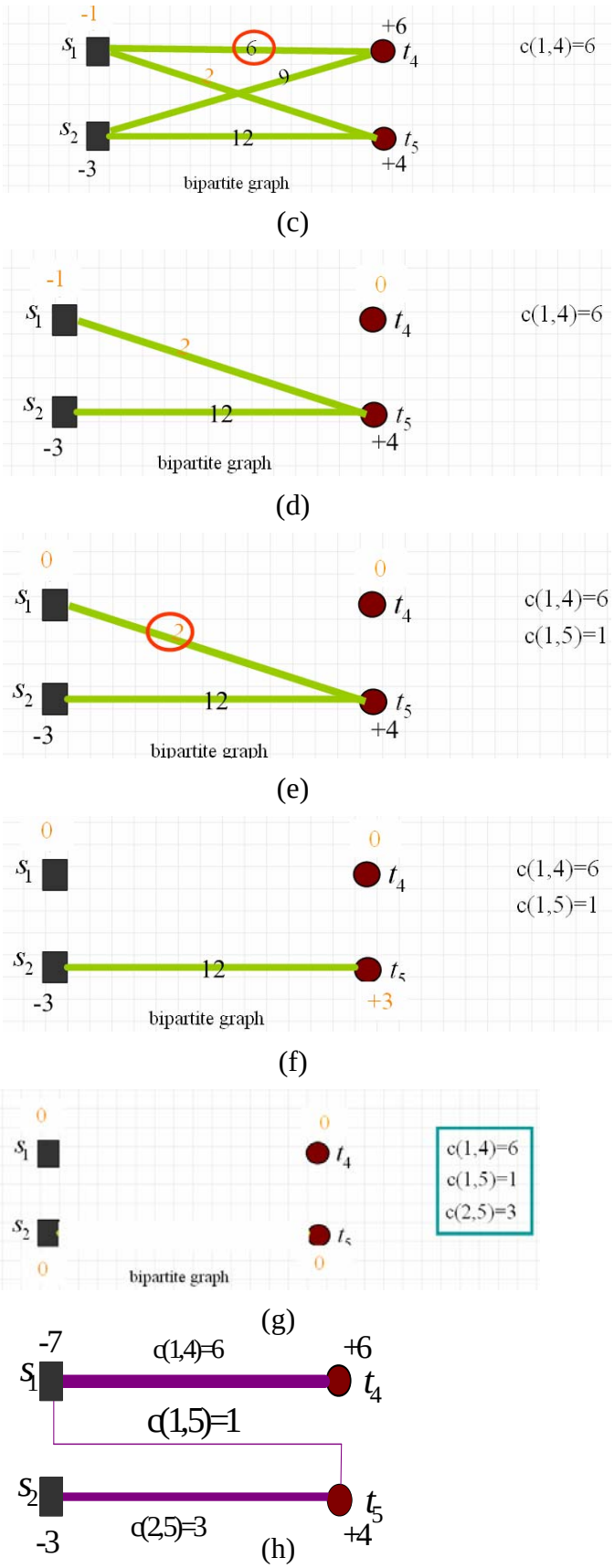


Figure 3. Bipartite graph for the graph method.

IV. Experimental Results

Our greedy graph-based approach is implemented by using C++ language on an Intel Core2 Duo 1.87G and 1.86G machine having 3GB main memory. The objective of the problem is to minimize the total wiring area of the current-driven wire planning with Kirchhoff's law. Because we are lack of the benchmarks and source codes in [8][9][10][11], the different benchmarks, which contain the sources, targets and obstacles, are modified from papers. The minimal wire width set to be 1*um*. Because of the lack of the real data, the RMS current values of sources and targets are randomly determined within the user-defined range. Obviously, our graph approach reduces the wiring area with the obstacles. For all benchmark, the statistics such as the number of obstacles, terminals, sources, targets are shown in Table 1.

First, we explore the effective of our graph-based method for improvement on the total wiring area without and with the obstacles. The obstacle ratios of the chip are from 8.2 to 39.4%. To deserve to be mentioned, the huge ratio of obstacles appears in R5. But the additional wiring area is only 4%. In Table 2, compared to the results without obstacles, we observe that the additional total wiring area with obstacles is increased only 9.18% in average. Hence, the proposed method is stably planning the wiring area for analog circuit.

Second, we investigate the relationship between the distribution of the obstacles and the additional wiring area. In Table 3, the additional wiring areas of R2 and R3 are 18.6 and 4.0% while the ratios R_{ob} of R3 and R4 are 21.7% and 39.4%. It means that the benchmark with the large ratio R_{ob} does not lead to the large additional wiring area. In fact, the distribution of obstacles also plays the important role on the additional area. If most obstacles located at the regions with many sources and targets, the additional wiring area is large. Otherwise, the additional wiring areas are small if most obstacles are located at the border of the chip. Summary, the distribution of the obstacles and the ratios R_{ob} play the same important role on the additional wiring area.

Finally, to avoid the interference between the obstacles and the wire, the proposed method reserves the dead-space for all obstacles. Hence, the benchmark, r1, is taken as the example. The results of wire planning are shown in Figure 4. The results without obstacles are shown in Figure 4(a). Most of the wires go straightly without the less number of bending. The results with the obstacles are shown in Figure 4(b). We observe that most of wires have many number of bending due to the huge number of obstacles. Figure 4(c) show the space between the obstacles and the wires. The proposed method indeed reserves the user-defined space to improve the interference.

V. Conclusions

In this paper, we propose the graph-based method which determines the proper widths for all wires to avoid the electromigration while minimizing the total wiring area. First, the reservation space technique is used to reduce the interferences between the obstacles and wires. Second, the graph-based method are utilized to determine the topology among the sources and targets according to circuit information after the greedy method is used to generate the feasible routing path with obstacles. Compared to the results without obstacles, our graph-based method leads to additional total area by 9.18% in average.

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Table 1. Benchmark circuits.

circuit	*No. of obstacle*	R_{ob}	*No. of terminal*	*No. of source*	*No. of target*
R1	10	8.2	10	3	7
R2	10	21.7	50	16	34
R3	10	39.4	70	23	47
R4	10	29.2	100	33	67
R5	300	10.7	200	66	134

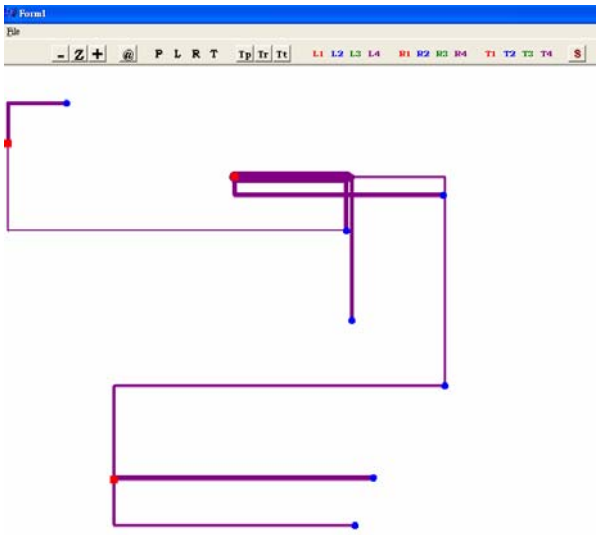
***Rob* denote the ratio between the obstacle and the chip area.**

Table 2. Comparison of the wiring area of greedy graph-based method *without* and *with* obstacle.

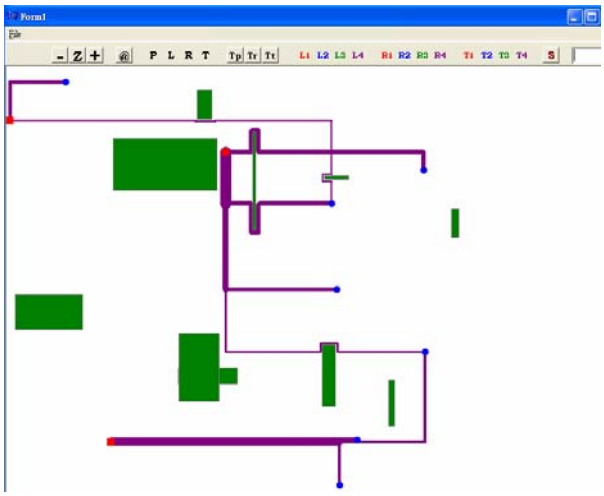
	I (WITHOUT)		**II (WITH)**		**Addition_area**
	Area1	***Time1***	***Area2***	***Time2***	100×(Area2-Area1)/Area1
R1	487160.0	0.0	520640.0	0.015	6.9
R2	1407820.0	0.015	1669400.0	0.046	18.6
R3	2415290.0	0.031	2510870.0	0.046	4.0
R4	2413740.0	0.031	2657820.0	0.078	10.1
R5	4098359.0	0.062	4356453.0	0.203	6.3
AVG	-	-	-	-	**9.18**

Table 3. Explore relationship between R_{ob} and additional area.

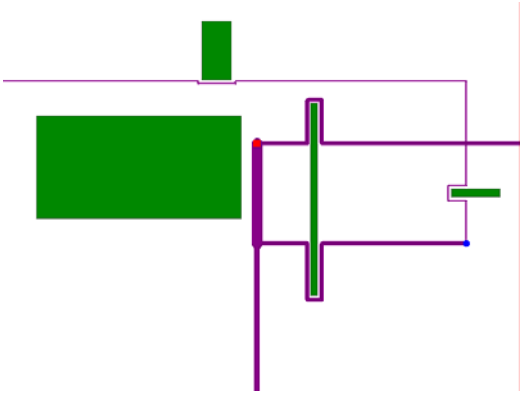
	R_{ob} **(%)**	**I (WITHOUT)**	**II (WITH)**	**Addition_area**
R1	**8.2**	487160.0	520640.0	**6.9**
R2	**21.7**	1407820.0	1669400.0	**18.6**
R3	**39.4**	2415290.0	2510870.0	**4.0**
R4	**29.2**	2413740.0	2657820.0	**10.1**
R5	**10.7**	4098359.0	4356453.0	**6.3**



(a) The wire planning without obstacles



(b) The wire planning with obstacle



(c) Local view of (a)

Figure 4. Wire Planning for greedy-based method (R1 circuits)