

On Achieving Better Signal Integrity in Area-Array Floorplanning by Minimal Decap Insertion

Chao-Hung Lu

Department of Electrical Engineer
National Central University
Taoyuan, Taiwan, R.O.C.
Email: chlu@ee.ncu.edu.tw

Hung-Ming Chen

Department of Electronics Engineering
National Chiao Tung University,
Hsinchu, Taiwan
Email: hmchen@mail.nctu.edu.tw

Chien-Nan Jimmy Liu

Department of Electrical Engineer
National Central University
Taoyuan, Taiwan, R.O.C.
Email: jimmy@ee.ncu.edu.tw

Abstract— With technology further scaling into deep submicron era, more components can be placed onto one chip (System-on-chip, SoC). However, the same scaling brings the design difficulties, among which signal integrity is one of the most important issues. Although flip-chip and area-array architectures have been proposed to strengthen the integrity, we still need careful planning in SoC designs. Power supply noise problem is getting worse due to serious IR-drop and simultaneous switching noise, and decoupling capacitance (decap) insertion is commonly applied to alleviate the noise. There exist some approaches to addressing this issue, but they suffer either from over-design problem or late decap insertion during design stage. In this paper, we propose a methodology to insert decap in a more efficient and effective way during supply noise driven floorplanning in area-array designs. The experimental results are encouraging. Compared with other approaches in [13] and [10], we have inserted enough decap to meet supply noise constraint while others employ more area.

I. INTRODUCTION

As VLSI technology enters the nanometer era, signal integrity become an important issue in the modern VLSI design. Basically, the integrity problem can be categorized in the signal noise issue and the power supply noise issue. In a modern low-power chip design, the supply voltage is continually dropped to reduce the power consumption. As a result, power supply noise becomes first order effect. Since the resistance of the interconnect would consume the energy of the power, power/ground (P/G) topology [7] [9], wire sizing [11] [3] could influence the voltage drop in the chip. In [9], Singh et al. use locally regular and globally irregular grids to optimize P/G design.

Employing decoupling capacitances (decap) has been a commonly used approach to reduce this kind of noise. Since manufacturing techniques continuously develop into the next generation, the gate oxide thickness is continually reduced. This results in the importance of the decap placement and sizing in digital chip design. In [13] and [10], they use decap insertion methods to improve power supply at floorplan level. Because some physical factors, such as the current of VDD pins would be durably supplied when the chip is turned on, are not considered, the decap budget could be conservatively computed and the floorplan area would be overly increased. Besides [13], [12] proposes a two-step decap insertion method to improve power supply noise in placement level. This method includes one prediction method and one correction method. In prediction step, the required decap is pessimistically estimated.

In correction step, the decap size is continually reduced until an appropriate size is obtained. We believe that it is better to insert decaps during floorplanning since the floorplanning stage is early for flexible changes in layout, while a better model to calculate decap budget is needed.

Due to recent high-performance IC manufacturing, the flip-chip and area-array architectures are applied, therefore the packaging issue should be accounted for in floorplan design. In [2], authors provide a power bump allocation method to effectively reduce the distance with from the supply voltage nodes to modules, thus reducing power supply noise. However, without decap insertion, resultant floorplans will still suffer from supply noise violations. Therefore, one simple and effective way to insert appropriate size of decap is to place the high current consumption module away from another high current consumption module in floorplanning. For the floorplan representation, Guo et al. [4] first propose an O-tree representation to maintain the adjacent relation for each block. To obtain a better floorplan result and less runtime program, [1] proposes a B*-tree floorplan representation to represent a floorplan structure. Recently, [10] develops a DBL representation to plan all modules and also integrate the decap insertion into floorplanning.

In this paper, We have developed a two-step methodology to reduce and suppress noise at the floorplan level, as shown in Fig.1. First, we use a noise-driven floorplan algorithm to suppress the noise. For each block, we consider the worst case current consumption. The power supply noise would be substantially increased when two high current consumption blocks are placed at the adjacent locations. Therefore, high current consumption blocks are not abut in our floorplan algorithm. The second step is the decap insertion method. We use a Noise-driven Decap Planning with Minimum Area Insertion (NDP_MAI) algorithm to reduce the noise after floorplanning. In this step, given an initial compacted floorplan and the current consumption for all blocks, the NDP_MAI algorithm is to use less decap budget and extensive floorplan area to determine the locations of the inserted decaps for each block to satisfy the noise constraints.

The rest of the paper is organized as follows. Section II presents the problem formulation. Section III describes our noise estimation method, decap budget computation. The floorplanning approach and decap insertion algorithm are presented in Section IV. Experimental results are shown in Section V. We conclude the paper in Section VI.

II. PROBLEM FORMULATION

In the traditional chip design, the decap insertion method is used to solve the power supply noise problem after the routing level . In

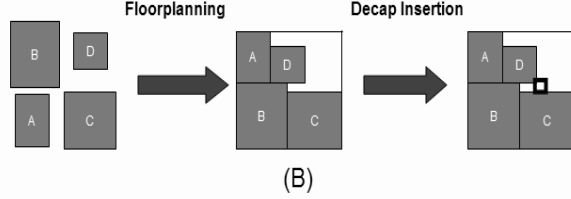
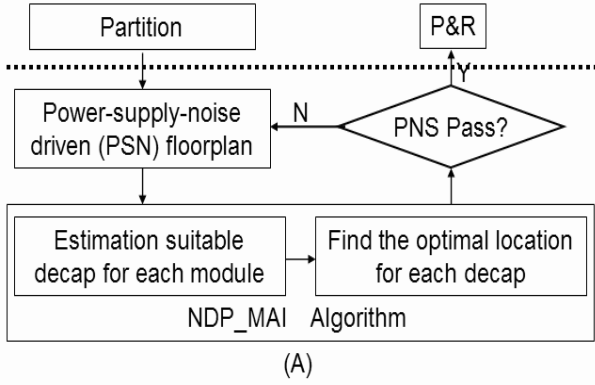


Fig. 1. Using a two-step approach that includes a PSN driven floorplanning algorithm and a decap insertion algorithm to improve the power supply noise before routing level. (A) The flow chart of our methodology. (B) The illustration of steps.

this paper, we propose to solve this problem in early design stage. Given a set of blocks, B_1, B_2, \dots, B_m , current consumption, I_{gen}^i and I_{max}^i , of each block $B_i, 1 \leq i \leq m$, the locations for each VDD source and the noise constraint for each module, find a feasible solution such that each block B_i obtains appropriate and minimal decap budget size DBS_i , and minimum penalty area when DBS_i is inserted.

III. POWER ESTIMATION MODEL AND SIGNAL INTEGRITY ISSUES IN AREA-ARRAY DESIGN

In this section, we describe our power delivery model and noise estimation model used in this paper.

A. Power Delivery Model and Noise Estimation

In this paper, the power source distribution is based on the area-array architecture. The area-array architecture is a mesh structure, as illustrated in Fig.2. In designing chips, the I/O location will seriously affect the performance. If the area-array architecture is used in the chip, the distance from the I/O location to the connection point of the model would be substantially decreased and the performance would be significant improved. Therefore, the area-array architecture is extensively used in the high-performance chip. Based on the area-array architecture, the power source of each module only considers four VDD sources – right-top, right-down, left-top and left-down – and other VDD sources are ignored. To reasonably simplify the power delivery estimation, only the shortest paths and the second shortest paths be considered in our model. In [13], they have shown that it is within 10% error bound if we only consider the shortest paths and the second shortest paths to simplify our estimation model. According to the preceding description, the noise calculation of each module can use Kirchhoff's voltage law to represent as follows:

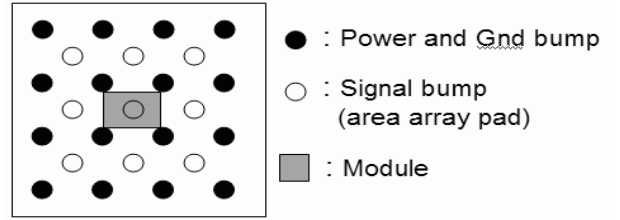


Fig. 2. Area-array footprint SoC. The Vdd and Gnd bumps are uniformly distributed across the die with signal bumps in fixed interspersed locations.

$$V_{noise}^{(k)} = \sum_{P_j \in T^k} i_j R_{P_{jk}} + L_{P_{jk}} \frac{di_j}{dt} \quad (1)$$

where $V_{noise}^{(k)}$ denotes the power supply noise at module k , P_j denotes the path from VDD to node j , T^k denotes the union of shortest paths and the second shortest paths, $R_{P_{jk}}$ denotes the resistance of P_{jk} , $L_{P_{jk}}$ denotes the inductance of P_{jk} and i_j is the current flowing along path P_j .

B. Decoupling Capacitance Budget Computation

Here we introduce the computation methodology for the suitable decap budget of each circuit module. Our computation methodology is based on the difference between the maximum and general current consumption for each module. We use a simple example to explain our computation method. The current consumption of module k in the general condition is defined as $I_{gen}^k, k = 1, 2, \dots, M$ and the maximum switching current of module k is I_{max}^k . For simplicity, the switching current waveforms are modeled as triangles as shown in Fig.3.

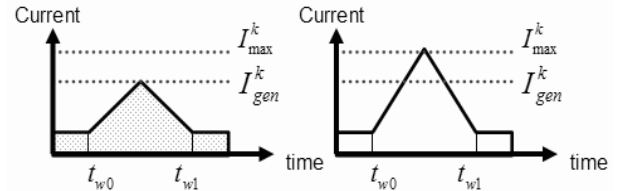


Fig. 3. Switching current consumption profile of module k . I_{gen}^k is only supplied by VDD pins and I_{max}^k is supplied by VDD pins and a decap budget.

The current consumption of the module in the general condition is only supplied by VDD pins, the maximum switching current can be supplied by VDD pins and vicinal decaps in a correct chip. Therefore, let C^k be the decap required for circuit k and Q^k is the amount of electric charge of the C^k . Q^k is given by the following equation (based on the model shown in Fig. 3):

$$Q^k = \int_{t_{w0}}^{t_{w1}} I_{max}^k(t) dt - \int_{t_{w0}}^{t_{w1}} I_{gen}^k(t) dt \quad (2)$$

where t_{w0} is the start time and t_{w1} is the finish time when the target module is in operational mode. The electric charge can be converted to the slicion area of the capacitance fabrication as follows:

$$C^k = \frac{Q^k}{V_{con}} \quad (3)$$

TABLE I
CAPACITANCE CALCULATED USING DIFFERENT APPROACHES. WE HAVE SET THE DROP VOLTAGE BIGGER THAN 2.46V. IF WE USE [13] TO COMPUTE THE REQUIRED CAPACITANCE, THE OVERLY CAPACITANCE IS REPORTED.

Method	Capacitance	Drop Voltage
Initial	0pF	2.44V
[13]	112pF	2.4715V
Equation(2)	96pF	2.4609V

$$S_{decap} = \frac{C_{decap}}{C_{ox}} \quad (4)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (5)$$

where V_{con} is the noise constraint of the voltage, C_{decap} is the decap budget and S_{decap} is the silicon area of C_{decap} . We use SPICE to verify our model (2) and compare with [13]. In our experiment, the supply voltage is set to be 2.5V and the power supply noise limit is set to be 0.04V. The experiment result is shown in Table I. It is obvious that the model we propose can obtain less required decap, while [13] conservatively estimate the decap budget.

IV. POWER SUPPLY NOISE AWARE FLOORPLANNING WITH MINIMAL DECAP INSERTION

In this section, we describe our floorplan method, floorplan space classification and decap insertion algorithm used in this paper.

A. O-tree Based Power Supply Noise Aware Floorplanning

Among various floorplan representations in Sequence Pair [8], B*-tree [1], O-tree [4], TCG [6], CBL [5], and DBL [10], we have adopted O-tree representation as our engine for supply noise driven floorplanning due to its strong adjacent module relation. If two high current consumption blocks are placed at the adjacent location, the power supply noise problem will get worse, and the performance of the chip will be reduced. Because O-tree representation[4] can maintain the adjacent relation for each block, we can use this representation to avoid this problem. In our approach, two transformation operations, *Delete* and *Insert*, are applied to obtain a new O-tree:

- *Delete* : Delete a set of blocks
- *Insert* : Insert a set of blocks

Those operations are different from the operations in original O-tree floorplanning algorithm. We have modified them so that they can be more useful in our framework. We use Fig. 4 to explain. If we use original operation to change the resultant floorplan, the high current consumption module may be placed in the adjacent location as shown in 4(A). If we use modified operations, the high current consumption module can be placed differently, as shown in 4(B).

To be more specific, we use an example to explain the *delete* operation. Before explanation, we briefly review the O-tree representation. In the O-tree representation, it use a horizontal tree structure and a vertical tree structure to express those operations. In Fig.4, the horizontal tree of O-tree representation is set as (0011000111,HLIJK) and the vertical tree is set as (0010101101,HIJKL), where the first half of the representation denotes the horizontal(vertical) relation and the second half of the representation is

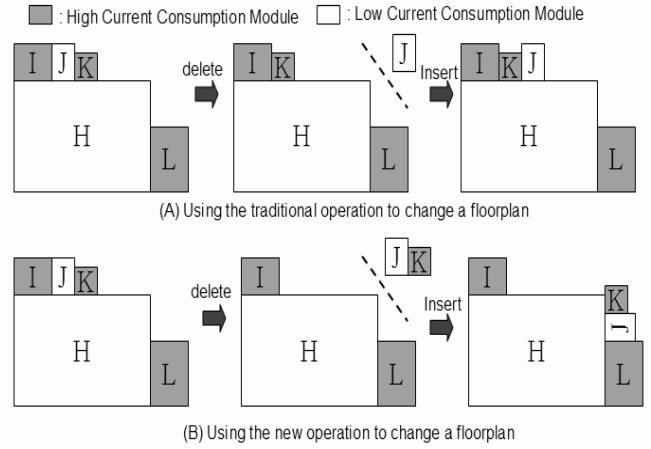


Fig. 4. The illustration between the usage of operations in original O-tree and our approach.

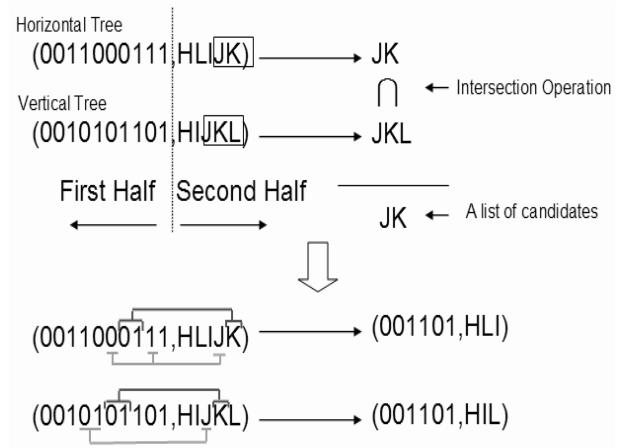


Fig. 5. Using new *delete* method to delete the module J. First, the candidate list can be obtained by applying Intersection Operation. Second, the original O-tree representation is modified until the list is not shown in the O-tree representation.

the order list of blocks. If the module J is selected to delete, we will obtain the delete module list from the parts of the second half representation, using the intersection operation in two trees, from the delete module to the last module, such as $JK \cap JKL$. Then we modify the original O-tree representation according to the result of the intersection operation, until the list is not shown in the O-tree representation. The illustration is shown in Fig.5. The *Insert* operation can be divided into three parts: (1) find all possible locations; (2) compute cost; (3) choose optimal location. We use a simple example to explain the *Insert* operation. First, all possible locations are found as shown in Fig. 6(A). We define the possible locations as the left-down corner of the empty space in current floorplan.

As shown in Fig.7, the area of the floorplan is possibly increased when the module J is inserted in the floorplan. Hence, in our cost function, it considers the floorplan area and the local current consumption. The cost function can be represented as follows:

$$C_a = D_1(A_{new} - A_{original}) + D_2(I_a + I_b + I_c - I_{th}) \quad (6)$$

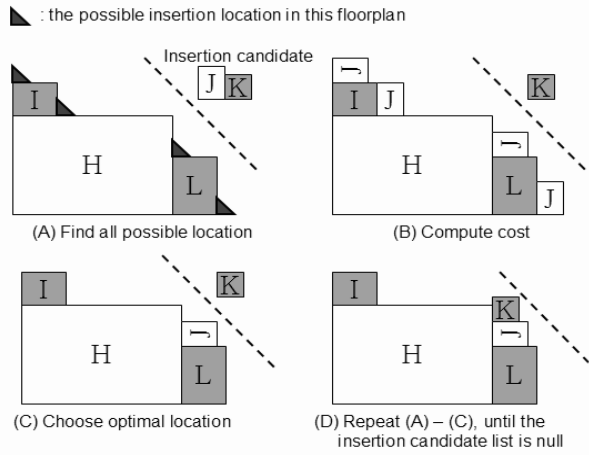


Fig. 6. Using new *insert* operation to insert all candidate modules.

where C_a denote the cost when the module A is inserted in this location, D_1 and D_2 are the weights, A_{new} is the area of the floorplan after the module is inserted, $A_{original}$ is the original area, I_a denotes the current consumption of the module a , and I_{th} denotes the threshold value for local current consumption. D_2 is to set a large value for penalizing high local current consumption. The describe of the floorplan algorithm as follows:

Power Supply Noise Aware Floorplan Algorithm

Input : A compacted floorplan , F , with the current consumption for each block

Output : A compacted floorplan , F , that two continuous high current consumption blocks could not placed together

begin

Set *Temperture* and *Final_Temperture*;

while *Temperture* > *Final_Temperture*

Random choose one block , B_x , from F ;

Using new **Delete** method to delete B_x ;

All deletion blocks are added into a candidate list;

while the candidate list is not NULL

Random choose one block , B_y , from the list;

Using equation (6) and new **Insert** method to insert B_y ;

Delete B_y information in the list;

end

$\Delta C = Cost(New\ Floorplan) - Cost(Floorplan)$;

if $\Delta C < 0$

Floorplan = *New Floorplan*;

else

if ($Random(0, 1) > e^{\frac{\Delta C}{Temperture}}$)

Floorplan = *New Floorplan*;

end

Cooling(Temperture);

end

end

B. Identification of Space Priority for Decap Insertion

The space in a floorplan could be divided into three types: the extensive space, the empty space, and the available space. The edge of the extensive space and the critical channel are the same. In Fig. 8, the horizontal critical path is $B \rightarrow C$, the critical channel is the

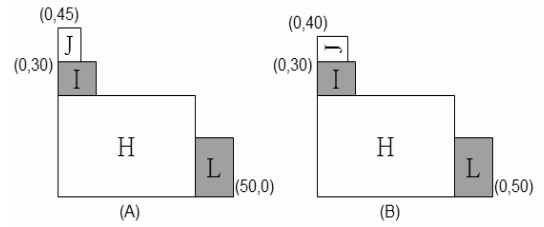


Fig. 7. One module must be inserted for two times at the same possible locations since the costs may not be the same for rotation.

edge between Block B and C. If one capacitance is inserted in the extensive space, the insertion operation will increase floorplan area as shown in Fig.8. In Fig. 8(A), the hollow square denotes one capacitance block and the channel space among B and C is the edge of the extensive space. If one capacitance block is inserted in this space, the circuit block and capacitance block must be moved as Fig 8(B). The area of the floorplan is then increased.

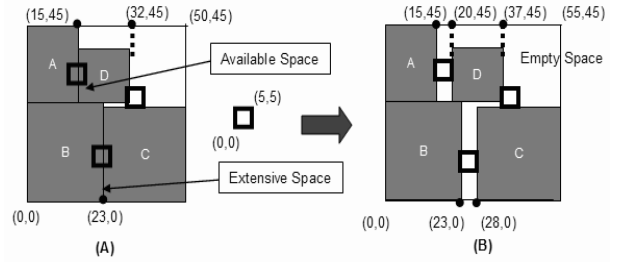


Fig. 8. When the decap is inserted into the different space in a floorplan, the area of the floorplan is possibly increased. (A) The area of the floorplan is $2250\mu m^2$ before the decap insertion. (B) The area of the floorplan is $2475\mu m^2$ after the decap insertion. The area is not increased when the decap is inserted into the empty space. If the decap is inserted into the available space, the area will be increased sometimes.

A channel space with the overlap edge of the empty room is called the empty space. If one capacitance is inserted in this space, all the blocks will be located on the original positions and the floorplan area will not be increased. The space in a floorplan is called the available space if it is not empty space or extensive space. If a capacitance is inserted in this space, the area of the floorplan would not be extended, but the location of some blocks could be changed. If one capacitance is inserted between the adjacent blocks A and D as in Fig. 8(A), the block D would be horizontally moved to its right. The result is shown in Fig. 8(B). Initially, the block A is the right block of the block D. After inserting decap, the right block of the block D is decap block and the area of the floorplan is not extended.

In summary, if the decap would be inserted in one floorplan and the candidate location of the decap has three type space could be selected – Available Space, Extensive Space and Empty Space, the priority of spaces must be defined. In this paper, we set the priority rule as follow :

Empty Space > *Available Space* > *Extensive Space*

C. Decap Insertion for Power Integrity

After obtaining one resultant floorplan from the first step, we will calculate required decap size for insertion. In order not to increase

the floorplan area excessively, we insert the decap with four smaller decaps instead of inserting one big decap in the extensive space. Given floorplan shown in Fig. 9, block D needs decap to supply the current consumption. First, we use equation (2)-(5) to compute the optimal decap sizing when the location of the decap and the VDD source of the module is separated. Second, the decap is cut apart into four smaller decap by the Manhattan distance from the VDD source to the power bump and the feasible region of each smaller decap is a rectangle from the connection point to the VDD pin. We compute the area cost of each space in the feasible region when the decap is inserted. If decap location and the connection point location are not close, the decap must add charge to compensate the consumption of the wire. The compensation methodology is shown as follows:

$$Q_{com}^k = Q^k + l \times c \quad (7)$$

where l is the distance from the space to the connection point and the c is wire capacitance per unit length. Finally, the minimum cost space be selected to inserted the decap. We called this methodology is NDP_MAI Algorithm and the describe as follows:

NDP_MAI Algorithm

```

begin
  while The power supply noise for block ,  $B_k$ , not estimated
    if  $I_{max}^k > I_{gen}^k$ 
      Using equation (2) – (5) to compute decap  $DBS_k$ ;
      The original decap is partitioned into four
      smaller decap based on the distance from VDD
      pins to the connection point of module  $k$ ;
      for each smaller decap
        Find the feasible region of the decap;
        Fix all the space in the feasible region;
        for each space in the feasible region
          Compute area cost when decap insert in
          this space;
        end
        Select the minimum cost space to insert
        decap;
      end
    end
  end

```

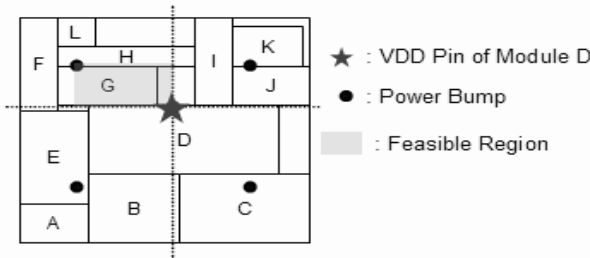


Fig. 9. The original decap budget is partitioned into four smaller decap. For each smaller decap, the feasible insertion region is from a power bump to the the VDD source. By this consideration, the smaller capacitance could be inserted into the trivial empty space and the charge time of the capacitance could be substantially decreased.

V. EXPERIMENTAL RESULTS

The proposed power supply noise aware floorplanning methodology and NDP_MAI algorithm have been implemented using C++ language on an AMD 3200 machine with 1G memory. The set of useful parameters of the formulation in the power delivery model is based on the $0.25\mu m$ technology and listed in Table II. Five MCNC benchmark circuits, apte, hp, xerox, ami33 and ami49, are used to test the performance of proposed methodology. The power supply voltage is 2.5V and the distance between two continuous VDD is $1000\Omega/\mu m$ and the power supply mesh is $333.3\Omega/\mu m$. The I_{gen}^k for the module k is $A_k \times D_c$, where A_k is area of module k , D_c is the worst case current density. The I_{max}^k is assigned as a random value to be $1.05I_{gen}^k \sim 2I_{gen}^k$. Since the MCNC benchmark include no noise constraint, the noise constraint is set to be 0.25V. In our experiments, the operation time t_{w0} and t_{w1} of the switching current waveform are set to be 0.3ns and 0.8ns. To compare our

TABLE II
PARAMETERS USED IN THIS PAPER, BASED ON $0.25\mu m$ TECHNOLOGY.

Parameters	Description	Value
r	Unit-length wire resistance	0.0125 ($\Omega/\mu m$)
c	Unit-length wire capacitance	0.4 ($fF/\mu m$)
l	Unit-length wire inductance	20 ($pH/\mu m$)
L_p	Package inductance per VDD pin	0.2 (nH)
R_p	Package resistance per VDD pin	0.5 (Ω)
j_s	Worst case current density	0.2 ($\mu A/\mu m^2$)

TABLE III
DECAP OBTAINED FROM OUR MODEL AND [13] ON THE SAME RESULTANT FLOORPLAN. THIS SHOWS OUR ESTIMATION NEEDS LESS DECAP TO SUPPRESS NOISE.

Circuit	Decap Budget (nF)	Decap Budget [13](nF)	Decrease Ratio
apte	7.01	13.46	47%
hp	1.65	2.75	40%
xerox	3.09	5.71	46%
ami33	0.08	0.27	70%
ami49	3.61	9.08	60%

TABLE IV
THE PEAK NOISE FOR ALL MODULES IN OUR APPROACH AND IN [13]. THE SOURCE OF THE DECAP BUDGET COMES FROM TABLE III. [10] DOES NOT PROVIDE PEAK NOISE INFORMATION.

Circuit	Our Peak Noise (V)	[13] Peak Noise (V)	[10] Peak Noise (V)
apte	0.25	0.24	N/A
hp	0.24	0.23	N/A
xerox	0.25	0.21	N/A
ami33	0.23	0.19	N/A
ami49	0.24	0.20	N/A

TABLE V

EXPERIMENTAL RESULT FOR MCNC BENCHMARK CIRCUITS. THE POWER SUPPLY NOISE CONSTRAINT IS SET TO BE 0.25V. THIS SHOWS THAT OUR APPROACH INSERTS LESS REQUIRED DECAP WHILE STILL MEETING DESIGN CONSTRAINTS.

Circuit	Modules	Area(μm^2) (Floorplan)	Area(μm^2) (Insert Decap)	Increase Area (μm^2)	[13] Increase Area (μm^2)	[10] Increase Area (μm^2)
apte	9	47761324	47780360	19036	469916	354000
hp	11	9940140	10097780	157640	317503	67000
xerox	10	20630210	20705216	75006	269374	144000
ami33	33	1241440	1245266	3824	390	11000
ami49	49	37504880	37659870	154990	218000	217000

method with [13], the decap budgets are listed in Table III. In [10], the experimental results only show the floorplan area and runtime. So we can not compare the decap budget with [10]. In Table III, it is clear that our computation methodology obtain more suitable decap budgets. The experimental results show that our decap budget obtained average improvement of 52.6%. The main reason is that [13] computed method ignore the supply current from VDD pins and the total charge is supplied by the decap when the power supply noise is occurred.

Table IV and V show the comparison of the experimental results between the other method and our proposed NDP_MAI algorithm. In Table IV, [10] does not provide the peak noise information in the experiment. In Table V, the experimental result of each benchmark circuit includes the area after floorplanning (Area(Floorplan)), the area after the decap budget insertion (Area(Insert Decap)) and the increase area after the decap insertion(Increase Area). The experimental results show that our proposed NDP_MAI algorithm use less penalty area to finish the decap insertion job in most cases and the noise constraint could be conformed in all MCNC benchmark at the same time.

VI. CONCLUSION

The techniques of floorplanning and decap insertion can be used to reduce the power supply noise in early design stage. Based on our framework, the suitable decap size is found. Furthermore, based on the analysis of the floorplan and space priority, the NDP_MAI algorithm is proposed to insert decap budget. Experimental results show that the proposed method can improve the increase ratio of the floorplan area when inserting decap. Our contributions presented in this paper are summarized as follows:

- We have developed a better noise estimation model and obtained less decap area, compared with previous approaches.
- We have adopted strong adjacent module relation O-tree representation as our engine for supply noise driven floorplanning, and successfully modified the primary operations *delete* and *insert* to be used in our framework.
- We have presented an algorithm to insert minimal decaps into a noise-guided resultant floorplan, with legalization embedded.

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