Pseudo-DCVSL Template for Power Awareness VLSI Circuit Design

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ABSTRACT

We design a pseudo-DCVSL dynamic logic by replacing the complemented network with a matched delay line rather than using the dual function of the target equation, whose low-power and small-in-area features are much better than the compared dual-rail DCVSL and dual-rail domino logics. Also, post-layout simulations are done to demonstrate all positive features and drawbacks of this circuit template; this template provides flexible techniques for low power design with stable performance. Besides, the layout area of the pseudo-DCVSL is always smaller than the compared logic families; for instance, the matched delay circuitry is much smaller than the complemented network in the dual-rail structure in general. 10 single-level logic equations from SIS library were selected and the test result shows more than 20% area reduction and 26% less power consumption in average. Furthermore, we simulate multi-level high fan-in AND gate and obtain remarkable result on both the area and power efficiency.

1: INTRODUCTIONS

There are many logic families applicable for the use of rail encoding; nevertheless, we are interested in understanding the influence on network selection and matching delay alternative in order to provide an effective technique in various applications.

1.1: DUAL RAIL ENCONDING

Dual rail encoding refers to the use of two wires for each data bit encoding. Each dual rail pair indicates both data and validity since the coding itself is an expression of data-dependent completion, in which the monotonic property of the logic families are discussed for the coding techniques needed in the circuit design [1].

1.2: DCVSL CIRCUIT

The DCVSL logic style was first introduced by IBM in 1984 [2], which consists of designing NMOS logic gates with two transistor networks, the first one generating the true output and the second one generating the complementary output to achieve the minimization of Boolean functions by algorithm [3] up to 2^N-1 input variables. The DCVSL circuit concept is that the f network or the f' network would be pulled down to ground one at a time and to indicate *On* on either T or F. The advantage is we trade area for the enhancement of the performance; DCVSL circuit shows about 4x better in performance compared to CMOS/NMOS primitive NAND/NOR logic families, and used about as twice as much in density than NAND/NOR logic. Also, DCVSL demonstrated a capacitance loading with a factor of 3X smaller than conventional static CMOS [4]. Moreover, DCVSL shows a monotonic property; we often take the monotonic characteristic in the DCVSL and use it for completion detection purpose [5].

1.3: DUAL-RAIL DOMINO CIRCUIT

The dual-rail domino circuit is the differential implementation of the traditional dynamic domino. This type of circuit exhibits a low delay; therefore, it is usually used in high-performance circuits. We may notice a similar circuit structure to DCVSL, which have two NMOS pulldown network two PMOS pairs driven by the clock in bringing the gate in the precharge or evaluation mode. The output inverters are placed to prevent race occurrence, and the weak feedback PMOS transistors are allowed reducing the charge-redistribution or known as charging sharing problem, and increasing the noise alleviation [6].

1.4: APPLICATIONS USING DCVSL CIRCUIT

Due to the nature of the DCVSL circuit properties, complementarities (i.e. using XOR-XNOR, AND-NAND, OR-NOR in one single circuit), and overwhelming efficiency in enhancing circuitry performance, many different applications favor this design technique. We may find DCVSL used for sequential designs such as fault-tolerant analyzer [7], fast dynamic circuits, and asymmetrical buffer circuitry [8]. Moreover, the DCVSL is also frequently used for self-timed circuit such as dual-rail design techniques, completion detection, pipeline structure [8], Dual-lock circuit [9] and so on. Since the applications are diverse and creative, it will be interested to know the circuit properties such as delay, power, logic density, device

complexity and compatibility by building a template with a possible automation tool.

2: ROPOSED TEMPLATE

We proposed a pseudo-DCVSL template which consists of three basic building blocks; they are the DCVSL primitive blocks, functional bock, and delay elements as illustrated in Fig. 1. The primitive block is a modified version of dynamic dual-rail logic structure. Functional block is a NMOS network implementing the desired logic functions we want. The delay element is used to replace the dual implementation of the functional block.

2.1: DCVSL PRIMITIVE BLOCK

The primitive blocks of our proposed DCVSL template are formed by the P1~P4, N1~N3, and 2 inverters as depicted in Fig. 1. When the PC ↑ arrives, outputs of both the T and the F are pulled high, consequently the OUT and OUTB will be pulled low after an inverter delay. This pre-charging state is hold until the PC ↓ arrived. In the mean time, all input signals can switch freely until the pre-charging phase terminates. When the PC ↓ is detected by the primitive block, the circuit enters the evaluation phase. Then, all input signals can only switching monotonically. Furthermore, we stress the strictness of the NMOS functional block used within the proposed template, of which it can only accept rising transition during the evaluation phase. The identical properties apply to conventional DCVSL logics as well.

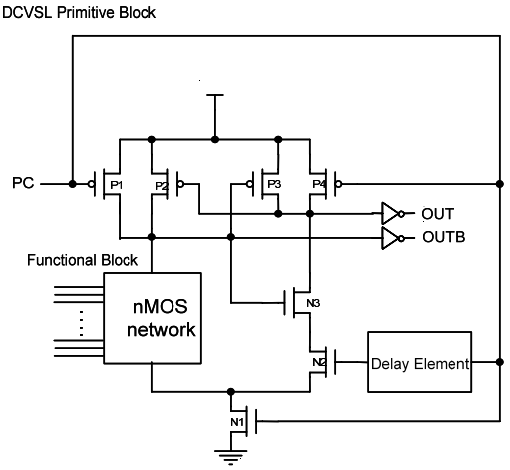

Fig. 1. Proposed DCVSL Circuit

The major difference between our pseudo-DCVSL and its conventional version is the duality of the functional blocks. Instead of implementing the dual structure, we use a much simpler configuration to mimic the complemented behavior. The circuitry consists of only 2 minimum-size NMOS transistors. N2 cooperates with the matched delay to form a pseudo complemented network while N3 disables this network when necessary.

The idea of pseudo complemented network is straightforward. The N2 will keep off-state until the postponed PC ↑ arrives, which is used to match the worst case evaluation delay of the functional block. If the N2 is turned on when N3 is still on, the completed network will pull down the pre-charged node F that lead to pulled-high on OUTB node. In the other words, the implemented function is evaluated to low for the given inputs. However, if N3 is already turned off before the N2 chances to pull down the complemented network, the function is said to be evaluated as high. Besides, N3 is also critical for the delay fault tolerance feature in our template, and we are going to discuss this in later section.

2.2: FUNCTIONAL BLOCK

The reason for using NMOS to implement the functional block is because most dynamic logic families tend to use NMOS for their evaluation networks, which shows fast switching than PMOS devices in general. For the single-level structure, our functional block is identical to the conventional DCVSL implementation. When the target logic function is too big to fit in the restrict transistor stack size, we can re-map the target logic function into a multi-level function. NMOS domino structure then is used to realize the decomposed multi-level function, except the last stage evaluation network that connects to the pseudo-DCVSL template.

The circuit area will be influenced by the choice of functional block implementation, indeed. Our pseudo-DCVSL implementation is always smaller than its conventional DCVSL counterpart. This is because our template provides dual behavior using matched delay instead of constructing complemented network. The reduced area cost property of the circuit becomes more observable when implementing larger logic equations. This property does not merely make circuit become smaller but also reduce the overall input loading, which will speed up the previous stages' evaluation. Furthermore, the area saving also reflects at the power saving nature because of the reduced switching power.

2.3: DELAY ELEMENT

With comprehensive critical path analysis of the target equation, we replace the complemented network using a set of simple NMOS devices (N2 and N3 in Fig. 1) with a matched delay line. The delay line can be as simple as a pair of inverters, which is good enough for implementing most primitive library cells from Berkeley SIS's libraries. When this kind of delay line is used, the inverter directly drives the N2 will be skewed to provide enough delay based on the worst case delay of the NMOS functional block. The invert driven by the PC signal is normally minimum-size, thus, the extra loading add to the PC is relatively small. Actually, with multi-level logic functions, the overall loading of the PC

signal in our template becomes substantially smaller than the DCVSL implementation.

3: EXPERIMENTAL RESULT

In order to confirm all the nice features we have expected, we select 10 primitive cells from Berkeley SIS's technology mapping libraries. We draw 3 different layouts of these logic equations using TSMC 0.35 μm technology. All these extracted circuits are tested with fan-out-of 1~4 loading under all simulation corners. Although we only shown the typical/typical corner result in this paper. We draw DCVSL, dual-rail domino, and proposed pseudo-DCVSL as layout templates. Thus, we could use the same functional blocks to plug-in each template, which ensures the comparison is fairly emulated and prevents additional specific optimization been applied to favor any of them.

3.1: DESINGN FACTOR: AREA, DELAY AND POWER

Table I and II are the measured area, delay, power consumption of the testing circuits. We are going to discuss the circuit area first. In the Table I, we can see that there is more than 20% area reduction in average for all testing cases. This area cost saving nature is observable from the replaced complemented network. The 20% improvement is not truly the average; it is only for the average of the listed cases. Remarkable area cost saving can be observed if we use larger circuits. We also learn that the decision of implementing the logic function or its complemented function has very little influence on the area reduction issue by observing these testing cases. This property allows designers or synthesis tools to be more focusing on the other two design factors (delay and power consumption) without concerning too much about the area overhead.

Selected Cases			Layout Area (um^2)			
SPEC	I	Lit	DCVSL	Domino	PD	PDC
and10	10	110	2047	1955	1320	1320
f01	12	91	1209	1026	1056	980
f02	12	99	1518	1376	1219	1081
f03	12	72	1110	1170	920	966
f04	12	97	1376	1344	1104	1012
f07	11	95	1584	1353	1035	1012

Table I Layout Area Comparison

Selected Cases			Power Consumption (uw)				Worst-case Evaluation Time (ps)			
SPEC	I	Lit	DCVSL	Domino	PD	PDC	DCVSL	Domino	PD	PDC
and10	10	110	406	397	273	442	1004	1045	734	526
f01	12	91	146	137	106	162	574	628	581	599
f02	12	99	153	149	110	164	573	653	581	590
f03	10	72	127	123	105	150	524	596	590	590
f04	12	97	153	147	110	164	600	665	581	597
f07	11	95	159	151	111	170	631	712	581	606

I: # of inputs Lit: # of literals PD: Pseudo-DCVSL(logic equation) PDC: Pseudo-DCVSL(complemented logic equation)

Table I I Power and Speed Comparison

Table II illustrates the worst case evaluation delays of three different dual-rail template styles. As we observe the table, we see the most circuits are faster than their conventional DCVSL counterparts in implemented complemented function in the NMOS functional block. The average speedup is about 15%, but this is not all we can get from speed. Based on all testing cases we have measured, the input loading of the proposed implementation is only a half of the other two styles, conventional DCVSL and dual-rail domino. The measured delay caused by the inputs load for the signals driving conventional DCVSL circuits is about 25% slower than when they drive the pseudo-DCVSL counterparts. If we include the input loading into account, the average overall speedup should be greater.

Low power consumption may be the most important design character for recent VLSI applications. Judging from the Table II, we learn that faster speed means more power. However, if low power is the most significant factor we are concerned, we should implement the original equations instead of its complemented functions. Of course, the circuits will slow down but not as much as in these testing cases. In most cases, they can still run as faster as the conventional DCVSL implementation. Actually, if we ignore the drawbacks caused by the non-optimized choice for area and speed, we can utilize this pseudo-DCVSL template to develop low power circuits easily. They also have the comparable performance of the conventional DCVSL counterparts with much smaller area.

3.2: DELAY FUALT ANALYSIS

Delay fault may occur when the matched delay fails to wait for sufficiently long period of time for the functional block to complete its evaluation phase. This failure may occur in many situations when the chip is fabricated such as process variations, signal coupling, noise, and so on. As long as the faulty circuit is caused by insufficient matched delay, the problem can be resolved easily but may not be very efficient. Adding more delay than the circuit actually requires is so-called safety margin. This simple technique has widespread utilization in recent digital systems; system clock signal is the most well-know application of this kind.

Delay fault is application dependent for the proposed template. Dynamic logics are much easier to be turn on than other logic families; therefore, when the value of the unwanted spike is greater than the device threshold voltage, which will result the circuit to failure. If the template is used as a low power version of DCVSL, the faulty signal transition caused by insufficient matched delay must not be seen by the dynamic logics which had driven. When the template is used as a self-timed wrapper, the timing constraint of this type will be a little bit loose. The data consumer in a self-timed system starts to evaluate its inputs when it receives completion signal from the data provider. Therefore, if the template can fix and restore the correct result before the completion signal

propagates to the asynchronous environment, the temporary faulty signal is negligible.

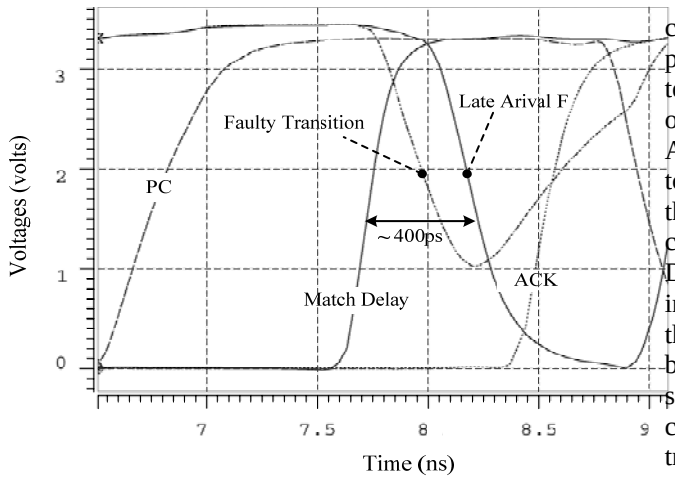

Fig. 2. Negative safety margin for delay fault tolerance

3.3: NEGATIVE SAFETY MARGIN

Negative safety margin is a special property of the proposed pseudo-DCVSL template. This is very different from the additional safety margin we add to the matched delay line explicitly. Negative safety margin appears only when the circuit needs it; however, additional safety margin will always add extra delay to the matched delay line. In order to make the template works, the network is pulled down by the matched delay so it should not operate before the pull down operation of the functional block occurs. In the ideal situation, we may use the delay line matches the worst-case evaluation time perfectly. In practical, designers will make the delay line longer than it supposed to be, that is because synthesizing a delay line using inverter chain is not a very reliable design in CMOS technology. If the extra delay is still insufficient to cover the delay variation, this is time for the negative safety margin come to rescue. This unique property is made possible by the N3 transistor in the Fig. 1. When the late arrival pull down operation of the functional block comes in, the N3 is going to be turned off. Thus, the discharged output node due to the delay fault is going to be restored to high. As long as the faulty signal does not propagate to the environment, the circuit still can work correctly. We have built a fault detection model to evaluate how much delay of this negative safety margin can handle properly. The post-layout simulation result is shown in the Fig. 2. Within a very conservative assumption, there are about 400 ps negative safety margin provided by the proposed template when TSMC 0.35 μm technology has used.

4: CONCLUSIONS

The proposed pseudo-DCVSL outperforms conventional DCVSL and dual-rail domino logics in power, area, delay, and capacitive loading. We use the test result in the circuit template and provide desirable options when designing the low-power controller circuit. Although the circuit performance can be degenerated due to the extra safety margin added to the matched added to the matched delay, the testing cases still shows a comparable dominant performance with the compared DCVSL and dual-rail domino counterparts since the input loading is only half of its original after removing the complemented network. Last, the performance can be further improved by aggressively using the negative safety margin nature of the proposed template. For a conservative design, this positive feature can also be treated as a freebee for delay fault reduction property.

5: REFERENCES

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