Reduction of Test Power during Test Application in Full-Scan Sequential Circuits with Multiple Capture Techniques

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ABSTRACT

In this paper, we propose a multiple capture approach to reduce the peak power as well as average power consumption during testing. The basic idea of the proposed approach is to divide a scan chain into a number of sub-scan chains, and only one sub-scan chain will be enabled at a time during the scan shift or capture operations. To efficiently deal with the "capture violation problem", we develop a test pattern insertion method to solve this problem. To reduce the number of patterns to be inserted, a scan chain partition method by exploiting don't care responses and a test pattern ordering method are also developed. The proposed approach can be easily implemented for any large full-scan sequential circuits. Experimental results for large ISCAS'89 benchmark circuits show that our approach can reduce the peak power and average power dissipation during testing significantly.

1. Introduction

Circuits are often designed to operate in normal and test modes. During test mode, the switching activity of nodes is often several times higher than the switching activity during normal mode. Hence, the power dissipation in test mode is significantly higher than in normal mode, and it may lead to circuit damaged during test application [3]. Generally, the test power dissipation consists of both scan and capture power dissipation, which is significantly higher than normal power dissipation. For conventional full scan scheme, the peak power are often occurred at the capture cycle due to responses are captured in all scan cells at the same time, or at the last scan shift cycle due to the values of primary inputs are changed at the instance of time. Hence, forcing the sub-scan chains to scan shift or to capture response at different cycles can help to reduce the peak power greatly.

Previous work for reducing power dissipation have been focused mostly on reducing the average power during test application, which are based on three major techniques: ordering techniques[5, 6, 7, 8], input control techniques[9, 10], and circuit modification techniques [11, 12, 13, 14]. Only a few work has been done on reducing the peak power. In this paper, we approach a simple but efficient multiple capture method to reduce the peak as well as average power during testing. The proposed approach allows only one sub-scan chain enabled at a time during scan shift or capture cycles, thus the average and peak power dissipation can be reduced. To make the multiple capture technique workable, we have developed a pattern insertion approach to solve the capture violate problem which is often occurred in multiple capture technique. Besides, to reduce the number of patterns inserted, we also develop a sub-scan chain partition approach by analyzing don't care response bits to partition the scan chain into don't care bit sub-scan chain (DCS) and care bit sub-scan chain (CS). After the scan chain has been partitioned, the corresponding test vectors are re-ordered into 2 groups, one are for single capture and the other are for multiple capture. In the single capture group, we further divide this group into 2 test sets "Set1" and "Set2". The test patterns in Set1 are all with don't care bits in sub-scan chain DCS, thus the test data in DCS only has to be shifted in once. For the next pattern of Set1, only sub-scan chain CS has to shift-in the test data because the test data in DCS can be reused. Therefore, if we can obtain more test patterns in Set1 then the test application time can be reduced more efficiently. For the multiple capture group, we combine the test pattern insertion method to get the test set "Set3". Finally, the complete test set contains 3 test sets, which are Set1, Set2 and Set3, respectively. More importantly, our proposed method is very simple and suitable for designers to implement for any large full scan-based sequential circuits.

The reset of this paper is organized as follows: In section 2, we analyze the power dissipation model of a CMOS circuit and capture violation problem. The detailed description of the proposed method is shown in section 3. Section 4 presents the experimental results. Finally, Section 5 concludes this paper.

2. Background

2.1 Power Dissipation Model

Power dissipation in a CMOS circuit can be classified into static power and dynamic power. The static power dissipation is caused by leakage current or other current drawn continuously from the power supply, and the dynamic power dissipation occurs during output switching because of short-circuit current, charging and

discharging of load capacitance. Generally, the power distribution in a CMOS circuit, the static power dissipation and short-circuit power dissipation contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs [4]. Therefore, the dynamic power dissipation takes the dominant part of power consumption for existing CMOS technology.

If the gate is part of a synchronous digital circuit controlled by a global clock, it follows that the dynamic power P_d required to charge and discharge the output capacitance load of every gate is given by

$$P_d = 1/2 \times C_{load} \times \left(V^2{}_{DD} / T_{cyc}\right) \times N_G$$

Where C_{load} is the load capacitance, V_{DD} is the supply voltage, T_{cyc} is the global clock period and N_G is the total number of gate output transitions (0→1 or 1→0). The vast majority of power reduction techniques concentrate on minimizing the dynamic power dissipation by reducing one or more variables of P_d. The supply voltage V_{DD} is usually not under designer control and global clock period T_{cyc} or more generally. Thus, node transition count (NTC) is used as a quantitative measure for power dissipation throughout the paper.

2.2 Capture Violation Review

Capture violation is a mainly problem in multiple capture techniques, when each sub-scan chain captures the responses at different cycles that may cause the data dependence issue. In the following, we use an example to illustrate this problem in details. Figure 1 shows that an example of capture violation scheme, clearly we can to see that there is a data dependence between scan cells S1 and S2 when they capture response at different cycles. For example, if S1 captures response before S2, the test stimulus bit in S1 may change the status and will cause G1 (logic gate 1) become undetected. On the other hand, if S2 captures response before S1, it may change the test stimulus bit in S2 and will cause G2 (logic gate 2) become undetected as well. Therefore, capture violation problem is a key problem for multiple capture techniques.

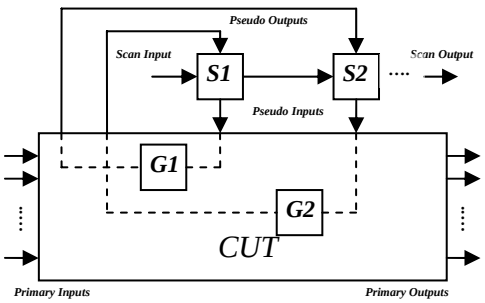

Figure 1. An example of capture violation scheme.

3. Proposed Method

3.1 Test Pattern Insertion

In this section, we use a simple example to illustrate the test pattern insertion method. In Figure 2, we assume that there is a circuit with 6 scan cells and are grouped into 2 sub-scan chains SC_1 and SC_2. In Figure 2(a), supposes there are 2 test patterns {*V_1, V_2 : AAA aaa, BBB bbb*} will be applied into the circuit, and there are 2 responses {*R_1, R_2: A"A"A" a"a"a", B"B"B" b"b"b"*} will be shifted-out from the circuit. Therefore, in the first step we will shift test pattern V_1 {*AAA aaa*} into SC_1 and SC_2, and then, sub-scan chain SC_2 will be captured first and the value will be replaced from current test pattern {*aaa*} to captured response data {*a"a"a"*} simultaneously. In order to avoid capture violation problem for next capture cycle for sub-scan chain SC_1, we have to re-shift test pattern value {*aaa*} into sub-scan chain SC_2 before execute the next capture cycle for sub-scan chain SC_1; hence a new test pattern $V_{1/}$ {*aaa*} will be added behind the V_1 {*AAA aaa*}. Same as above, the test pattern $V_{2/}$ {*bbb*} will be also added behind the V_2 {*BBB bbb*} as shown in Figure 2(b). Finally, in order to shift-out the last response data that we have to add an extra test pattern as *XXX*, the values must be either 111 or 000.

We now describe the test pattern insertion rule for our proposed method. The basic idea is to add a test pattern behind each original test pattern as shown in Figure 3. For example, assume that a scan chain is partitioned into *n* sub-scan chains and there are *i* original test patterns for circuit testing. Based on the rule of test pattern insertion, we have to add a new test pattern ($V_{1/}$) behind the original test pattern (V_1), which contains the test values of $\{V_{1SC_2}, V_{1SC_3}, ...V_{1SC_n}\}$. After that, another new test pattern ($V_{2/}$) will be added behind the original test pattern (V_2), which contains the test values of $\{V_{2SC_2}, V_{2SC_3}, ...V_{2SC_n}\}$. Hence, totally there are *i* new test patterns will be added into this test set.

The draw of the pattern insertion method is that it increase too many test patterns in the test set, thus the test application time will be increased greatly. The following shows the equation of test application cycles by using the pattern insertion method.

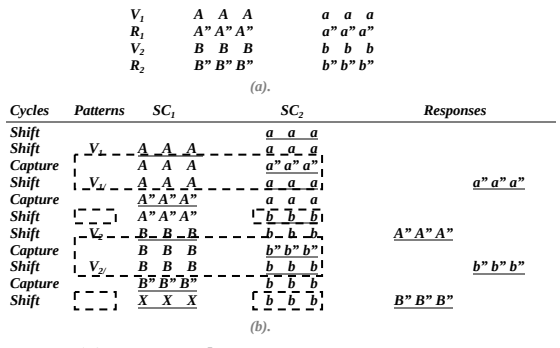

Figure 2(a) 2 original test patterns.
(b) sequence for test pattern insertion.

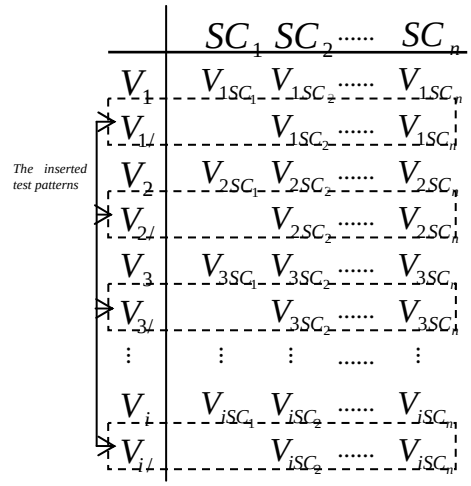

Figure 3. The rule of test pattern insertion

Test Application Cycles =

$$(DFF + (DFF\text{-}SC_1\_DFF) + n) \times i + SC_1\_DFF \quad (1)$$

DFF: Scan shift cycles for each original test pattern.

DFF-SC_1_DFF: Scan shift cycles for each new test pattern.

n: Capture cycles for each test pattern testing.

i: The number of original test patterns.

SC_1_DFF: Last scan shift cycles.

For example, we assume that there is a circuit with 9 scan cells and divide into 3 sub-scan chains. In Figure 4 (a), there are 3 test patterns *{V_1 – V_3 : AAAAAAAAA, BBBBBBBBB, CCCCCCCCC}* will be applied into this circuit, based on the test pattern insertion rule in Figure 3 that we can follow the procedure to generate the new test patterns as *$V_{1/}${AAA, AAA}*, *$V_{2/}${BBB, BBB}*, and *$V_{3/}${CCC, CCC}*.

Based on this rule, we can get the new test pattern set as shown in Figure 4(b), and the total number of increased patterns are 3 since i = 3. Hence, there are 3 test patterns will be added into original test set, and the total test application cycle is 57 ((9 + (9 - 3) + 3) × 3 + 3). Compared to conventional testing ((9 + 1) × 3 + 9 = 39), the proposed test pattern insertion method will take more 46.15% (57/39 - 1)%) test application cycles than conventional testing, the overhead of test application time is too much for this method. As the test application time overhead of circuit s5378 showed in Table 1, the test application time will be increased 49.21%, 74.91%, 89.14% and 99.56%, respectively, when 2, 4, 8 and 16 sub-scan chains are used.

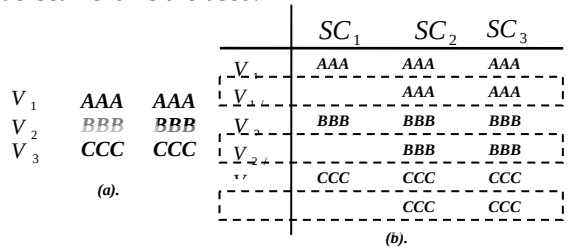

Figure 4 (a) Original test patterns
(b) Test patterns after test pattern insertion

Ckt	Conventional testing			Test pattern insertion			AC2 / AC1 (%)
	DFF	TP1	AC1	Sub-scan chain No.	TP2	AC2	
s5378	179	124	22499	2	124+ 124	33570	149.21
				4	124+ 124	39353	174.91
				8	124+ 124	42555	189.14
				16	124+ 124	44900	199.56

Table 1: Test application time overhead for s5378

3.2 Scan Chain Partition

Generally, there are many test cubes, i.e., test patterns and response data with don't care bits, which are usually generated by ATPG tool. Our basic idea is to analyze the don't care response bits and divide the scan cells into two sub-scan chains, which are don't care bit sub-scan chain(DCS) and care bit sub-scan chain(CS). For next, we use a simple example in Figure 5 to illustrate our basic idea. We assume that there is a response date set with don't care bits as showed in Figure 5(a), after the response data set is analyzed, we can obtain that there are 3 scan cells (S_1, S_3, S_7,) contain over 7 don't care bits if we perform a third of scan cells in the don't care bit sub-scan chain(DCS). Hence, the scan cells S_1, S_3 and S_7 will be put into DCS and others will be put into CS. The scan cell number of DCS and DS are 3 and 6, respectively. The partitioned sub-scan chain architecture is shown in Figure 5(b).

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
R_1	x	0	x	1	x	1	1	0	1
R_2	x	x	x	0	x	0	x	x	x
R_3	x	1	1	1	1	x	x	1	0
R_4	x	x	x	0	1	0	x	x	1
R_5	x	0	x	x	1	0	x	1	x
R_6	x	x	x	x	x	1	x	0	1
R_7	x	0	x	x	0	x	x	1	1
R_8	1	x	x	1	0	0	x	x	0
R_9	1	1	1	1	0	1	x	0	1
R_{10}	x	1	0	x	x	x	0	1	0
	8	4	7	4	4	3	8	3	2

Figure 5(a). A response data set with don't care bits

	DSC			DC					
	S_1	S_3	S_7	S_2	S_4	S_5	S_6	S_8	S_9
R_1	x	x	1	0	1	x	1	0	1
R_2	x	x	x	x	0	x	0	x	x
R_3	x	1	x	1	1	1	x	1	0
R_4	x	x	x	x	0	1	0	x	1
R_5	x	x	x	0	x	1	0	1	x
R_6	x	x	x	x	x	x	1	0	1
R_7	x	x	x	0	x	0	x	1	1
R_8	1	x	x	x	1	0	0	x	0
R_9	1	1	x	1	1	0	1	0	1
R_{10}	x	0	0	1	x	x	x	1	0

Figure 5(b).The sub-scan chain architecture after partition

3.3 Test Pattern Ordering

After the sub-scan chain DCS is identified, we have to further analyze that how many response data in DCS are all with don't care response bit, it means that these corresponding patterns can skip the capture operation

for DSC during testing. In Figure 5(b), there are 3 scan cells in sub-scan chain DCS, and there are 5 response data(R_2, R_3, R_5, R_6, R_7) are all with don't care bits in DCS, thus we can skip the capture operation for sub-scan chain DCS during these corresponding test pattern(V_2, V_3, V_5, V_6, V_7) in testing. The analysis result is shown in Figure 6.

Based on the analysis results, we have to order the corresponding patterns and divide them into two groups as showed in Figure 7, which are single capture and multiple capture groups. The single capture group contains 5 test patterns (V_2, V_3, V_5, V_6, V_7) and the multiple capture group contains another 5 test patterns (V_1, V_4, V_8, V_9, V_{10}).

	DSC			DSC			CS					
	S_1	S_3	S_7	S_1	S_3	S_7	S_2	S_4	S_5	S_6	S_8	S_9
R_1	x	x	1	V_1	x	0	x	1	x	1	1	x	0
R_2	x	x	x	V_2	x	x	x	0	0	0	x	x	x
R_3	x	x	x	V_3	x	1	x	1	1	x	x	1	0
R_4	x	1	x	V_4	x	x	1	0	1	0	0	0	1
R_5	x	x	x	V_5	x	x	1	x	1	0	x	0	x
R_6	x	x	x	V_6	1	x	0	x	x	1	1	0	1
R_7	x	x	x	V_7	0	x	x	x	0	x	0	x	x
R_8	1	x	x	V_8	1	x	x	0	x	0	0	x	0
R_9	1	1	x	V_9	1	1	1	1	0	1	x	0	1
R_{10}	x	0	0	V_{10}	x	1	0	x	x	x	0	x	x

Figure 6. Don't care bits analysis for DCS

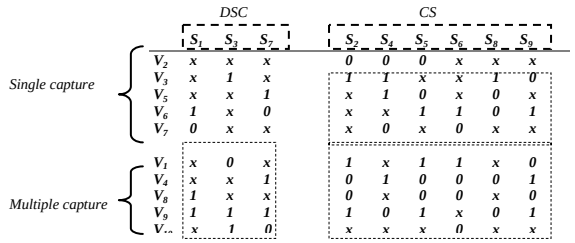

Figure 7. Test patterns ordering for single capture and multiple capture groups

Consider for single capture group. Some of test patterns in DSC may all with don't care bits. If so, these patterns can put into same test set called "Set1", and other patterns put into another set called "Set2". For our example showed in Figure 8(a), after the single capture group is divided that Set1 contains one test pattern(V_2) and Set2 contains 4(V_3, V_5, V_6, V_7) test patterns, respectively.

For Set1, we shift the test pattern into both sub-scan chain DCS and CS for one time only, and next, we just shift patterns into CS for capture operation because Set1 contains same test data for DCS. The equation of test application cycles for Set1 as follows:

Test Application Cycles = (DFF+1) + ((CS_DFF+1) × (Set1_TP-1)) … (2)

(DFF+1): First scan shift cycles for all scan cells and plus one capture cycle for CS.

(CS_DFF+1): Scan shift cycles and plus one capture cycle for CS.

(Set1_TP-1): The test pattern numbers of Set1, decrease one test pattern for first test pattern.

For Set2, each test pattern has to shift into both sub-scan chains DCS and CS, and plus a capture cycle for sub-scan chain CS. The equation of test application cycles for Set2 as follows:

The Application Cycles = (DFF+1) × Set2_TP…. (3)

(DFF+1): Scan shift cycles for all scan cells and plus one capture cycle for CS.

(Set2_TP): The test pattern number of Set2.

Based on the above explanation, Set1 takes the test application time less than conventional circuit testing, and Set2 equals. In other words, if we can obtain more test patterns in Set1 that the test application time can be reduced more efficiently. Therefore, we approach another method to add Set1 size is to determine 0's or 1's for don't care bits. We now use example in Figure 8(a) again, there are 4 Set2 test patterns (V_3:x1x, V_5 :xx1 , V_6:1x0, V_7:0xx) in DCS, we first assigning 0 into the don't care bits, and we can get results as V_3:010, V_5 :001 , V_6:100, V_7:000. After that, we find that there is a test pattern (V_7:000) can be moved from Set2 to Set1. Secondary, let us assigning 1 into the don't care bits, and get results as V_3:111, V_5:111 , V_6:110, V_7:011, we find that there are 2 test patterns (V_3:111, V_5 :111) can be moved from Set2 to Set1. Hence, assigning 1 for don't care bit is better than assigning 0 for don't care bit on this case. Figure 8(b) shows that Set1 and Set2 structure after the don't care bits are assigned to 1. However, the determined test patterns can reduce the test application time more efficiently than before, because the Set1 size is increased from 1 to 3 patterns.

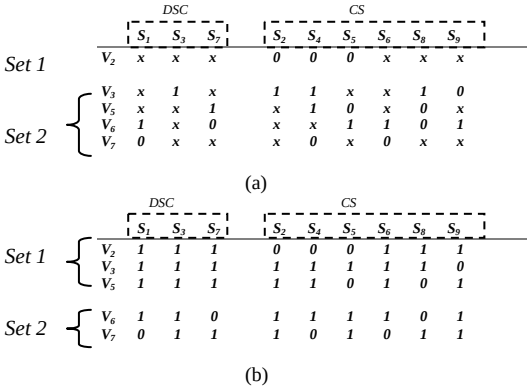

Figure 8(a).Divide the single capture group into Set1 and Set2.
(b).The test set of Set1 and Set2 after assigning 1to don't care bits.

For next, let us consider for the multiple capture group. We have to follow the test pattern insertion rule as mentioned in section 3.1 to generate a test set called Set3, which is shown in Figure 9. For the test application time calculation, Set3 will take more test application cycles than Set1 and Set2 because there are many test patterns are inserted into original multiple capture group. The equation of test application cycles for Set3 as follows:

The Application Cycles = ((DFF+DCS_DFF+2)× Set3_Org_TP) + CS_DFF …….. (4)

(DFF): Scan shift cycles for each original test pattern.

(DC_DFF): Scan shift cycles for each new test pattern.

(+2): Two capture cycles for DCS and CS.

(Set3_Org_TP): The number of original test patterns.

(DCS_DFF): Last scan shift cycles.

Finally, we have to assigning 1 for all the don't care bits because it can add the Set1 size, and we can get a

complete test set as showed in Figure 10, this test set contains 3 test patterns in Set1, 2 test patterns in Set2 and 8 test patterns in Set3.

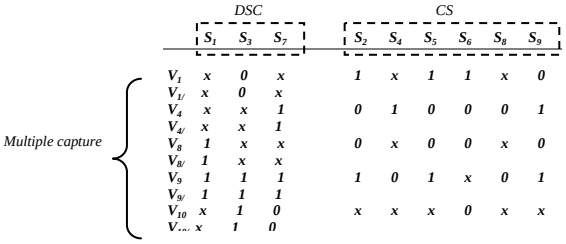

Figure 9. Test patterns insertion for multiple capture group

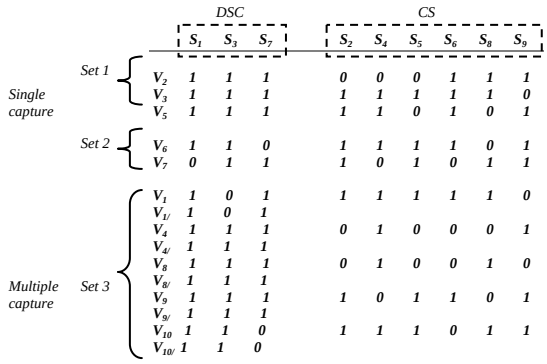

Figure 10. The complete test pattern set

3.4 The Proposed Architecture

The basic architecture of our proposed method is shown in Figure 11, the scan chain is divided into DCS and CS sub-chains, and only one sub-scan chain will be enabled at a time during scan shift or capture operations.

In the normal mode, the signal SE will be set to 0, and the signals CLK_DCS and CLK_CS are mapped to system clock. Thus all scan cells are activated in the normal condition.

There are 2 types of cycles in the test mode, which are scan shift cycle and capture cycle. During test mode, the signal SE will be set to 1 and 0 for scan shift cycle and capture cycle, respectively. Besides, the signals CLK_DCS and CLK_CS will be activated for sub-scan chains DCS and CS during scan shift or capture operations.

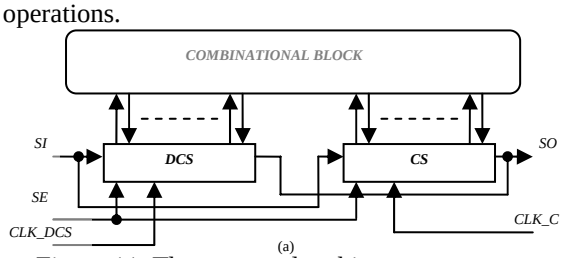

Figure 11. The proposed architecture

4. Experimental Results

The proposed method is implemented on eight largest ISCAS89 benchmark circuits, and used the node transition count (NTC) to estimate the percentage of power reduction. In this experimental, the test patterns are generated by Sytest ATPG tool "Turboscan".

Table 2 shows the experimental results of test application time overhead. The circuit name is shown in column 1. After the circuit name, the follow 3 columns "DFF", "TP1" and "AC1" give the number of flip-flops, the number of test patterns and the number of test application cycles for conventional scan test method, respectively. After that, the latter columns are defined for our proposed scheme. Columns "DCS_DFF" and "CS_DFF" give the flip-flop number of sub-scan chain DCS and sub-scan chain CS. The number of test patterns for Set1, Set2 and Set3 are shown in columns "TP2_Set1", "TP2_Set2" and "TP2_Set3, respectively. Column "AC2" gives the number of test application cycles. And then, column "1 or 0" stand for assigning 1 or 0 for don't care bits. The last column gives the result of test application time overhead. In this experimental, the increased test patterns of Set3 may increase the test application time. However, as the results show, for circuit such as s13207.1, the number of test application cycles of the proposed method is smaller than the conventional testing. It means that if we can get bigger size for test pattern set Set1, we may get a smaller test application time than the conventional testing.

The experimental results for power dissipation are shown in Table 3. Same as in Table 2, the circuit name is also shown in column 1, and the following 4 columns are defined for conventional scheme results. Columns "TP1" and "TC1" give the number of test patterns and the number of total transition counts. The maximum number of transition counts and average number of transition counts are shown in columns "PTC1" and "ATC1", respectively. For the latter columns, they are defined for our proposed scheme results. In columns "TP2" and "TC2", the number of test patterns and the number of total transition counts are given. And then, the columns "PTC2" and "ATC2" give the maximum number of transition counts and average number of transition counts, respectively. Finally, the last 2 columns are shown for the reduction results of maximum and average node transition counts. As this experimental results show, our proposed method can reduce maximum node transition counts and average node transition counts by 22.46% and 39.83% in average, respectively.

5. Conclusions

For multiple capture technique, it has often caused some side effects in order to deal with capture violation problem, either requires large hardware overhead to cause performance degradation or increase test application time. However, the proposed approach can reduce the peak power as well as average power dissipation during scan shift and capture operations, without requiring large hardware overhead. In addition, the proposed approach is very simple and easy to implement for any large full-scan sequential circuits without impacting the fault coverage.

Circuit	Conventional Scheme			Proposed Scheme						1 or 0	AC2 / AC1 (%)
	DFF	TP1	AC1	DCS DFF	CS_ DFF	TP2_ Set1	TP2_ Set2	TP2_ Set3	AC2		
s1423	74	40	3074	21	53	4	10	26+26	3562	0	115.88
s5378	179	124	22499	59	120	9	70	45+45	24668	1	109.64
s9234.1	211	167	35615	71	140	11	84	72+72	40018	1	112.36
s13207.1	638	270	173168	211	427	188	16	66+66	147492	0	85.17
s15850.1	534	151	81319	182	352	47	31	73+73	86124	1	105.91
s35932	1728	44	77804	546	1182	4	2	38+38	96406	1	123.91
s38417	1636	101	166973	553	1083	1	43	57+57	197998	1	118.58
s38584.1	1426	171	245443	462	964	40	7	124 +124	284375	1	115.86
									Average		110.91

Table 2: Experimental results of test application time overhead

Circuit	Conventional Scheme				Proposed Scheme				PTC2/ PTC1 (%)	ATC2/ ATC1 (%)
	TP1	TC1	PTC1	ATC1	TP2	TC2	PTC2	ATC2		
s1423	40	1298948	874	422	66	882807	637	247	72.88	58.53
s5378	124	21332386	2432	948	169	15108390	1830	612	75.25	64.56
s9234.1	167	83358204	4173	2340	239	53608078	3475	1339	83.27	57.22
s13207.1	270	427158023	6043	2466	336	2500772973	5194	1700	85.95	68.94
s15850.1	151	313806418	6826	3858	224	192600608	5728	2236	83.91	57.96
s35932	44	638074417	20058	8201	82	433333121	15894	4494	79.24	54.80
s38417	101	1576189013	19538	9439	158	1061492596	15044	5361	77.00	56.80
s38584.1	171	2012721068	17896	8200	295	1459958621	11240	5133	62.81	62.60
								Average	77.54	60.17

Table 3: Experimental results for peak and average power reduction

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